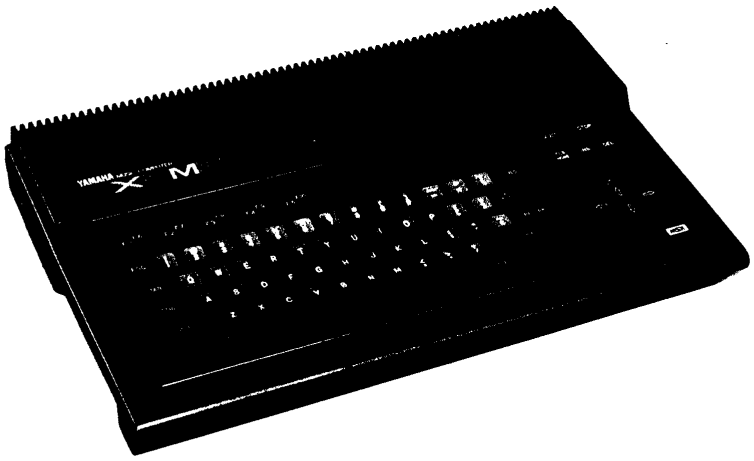
MUSIC COMPUTER

CX-5M II

SERVICE MANUAL



MSX

CX-5M II C
CX-5M II E
CX-5M II F
CX-5M II A
CX-5M II B
CX-5M II P

■ CONTENTS

008511

SINCE 1887 YAMAHA
NIPPON GAKKI CO., LTD. HAMAMATSU, JAPAN
0.99K-897 ㊞ Printed in Japan '86.6

ACCORDING TO AREA

YAMAHA MSX COMPUTER according to area, this manual refer to the
II, referring to all models. Where reference to particular model is called for,
rtaining to the area in question will be used. The different model numbers,
rtain, are as follows.

Canada ..... (NTSC)
CX-5MIIE ..... United Kingdom ..... (PAL-I)
CX-5MIIA .... Australia and New Zealand ..... (PAL-B)
CX-5MIIF ..... France ..... (PAL-G)
CX-5MIIB ..... Italy ..... (PAL-G)
CX-5MIIP ..... Spain ..... (PAL-G)

■ MSX COMPUTER A

There are different models of
computer as only the CX-5M
the specific model number pe
and the area to which they pe

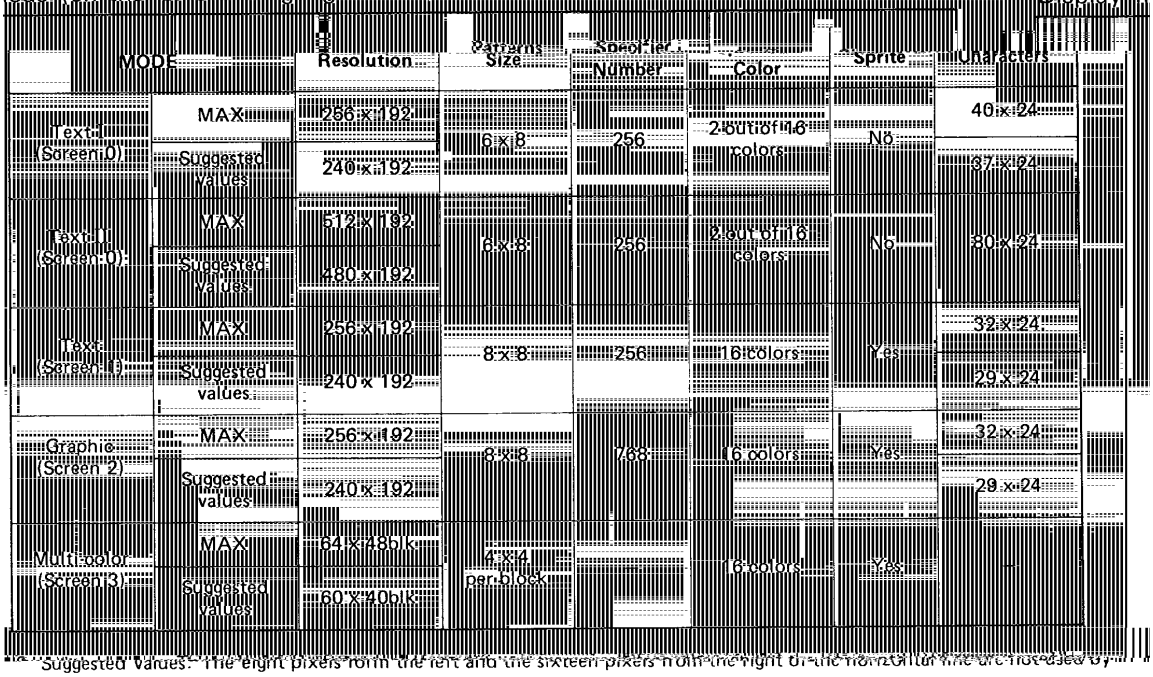
CX-5MIIC .....

EN DISPLAY

■ SCRE

ode (on the BASIC language mode)

Display



Suggested values: The eight pixels from the left and the sixteen pixels from the right of the horizontal line are blocked by the software.

■ SPECIFICATION

CPU

Type:	LH0080A (Z80A compatible)
Clock:	3.579545MHz
Wait:	1 wait in M1 cycle
Interrupt:	NMI-not used INT-accept interrupts from VDP and cartridge SLOT The interrupt mode is Z80 mode 1. The interval of the interrupt is 50Hz (NTSC: 60Hz).
Reset:	Power on reset and reset switch.

MEMORY

Main Memory:	128 Kbyte (128 Model)
(RAM)	64 Kbyte (64 Model)
BASIC ROM:	32 Kbyte (MSX1-BASIC)
Sub ROM:	16 Kbyte (for 80 Chara)
Video RAM:	16 Kbyte

VIDEO DISPLAY Video Display Processor (VDP)

Type:	V9938
Character Set:	256 alphanumeric and graphic characters
Color:	16 colors
Text mode:	SCREEN 0 or SCREEN 1
Capability:	24 lines by up to 80 columns (Software selectable)
Resolution:	256 x 192 pixels (non interlace)

INPUTS AND OUTPUTS

Keyboard:	Stroke type step sculpture keyboard. Alphanumeric and special characters . 48 Control and special effect keys . . . . 16 Cursor movement keys . . . . . 4 Function keys (programmable) . . . . 5 CAPS lock key with LED indicator
Cassette Interface:	8 pin DIN female connector Baud rate 1200/2400 BPS selectable by software, FSK format. With remote control (Cassette motor ON/OFF)
Printer Interface:	Standard centronics 8-bit parallel TTL logic level 14 pin female connector
Univarsal I/O Interface:	2 ports (JOYSTICK) 9 pin male connectors TTL logic level
Audio/Video Output:	1) MONITOR output RCA type pin connector CX-5MIIE, F, A, B, P PAL composite video output 75 ohm CX-5MIIC NTSC composite video output 75 ohm 2) SOUND output RCA type pin connector CX-5MIIC, E, F, A, B, P 8 octaves 3 tones + noise BEEP sound 3) RF output RCA type pin connector CX-5MIIC: NTSC (VHF3, 4) CX-5MIIA: PAL (VHF3, 4) CX-5MIIE, F, B, P : PAL (UHF36) 4) RGB output 8 pin DIN female connector CX-5MIIC, E, F, A, B, P 5) Color or Block/White switch Monitor and RF output used
Upper SLOT A, B:	SLOT 1, 2 50 pin MSX standard female connector
SIDE SLOT:	SLOT 33 60 pin edge card connector FM sound unit
BILT in ROM SOCKET:	SLOT 30 30 pin plug right ungle type

FM SOUND SYNTHESIZER UNIT

Number of Preset Voices:	46
Simultaneous Notes:	Up to 8 notes
Audio L/R Outputs:	−9 ± 2dB, 1.8kΩ RCA-pin jacks
MIDI IN/OUT:	5 pin DIN female connectors
Music Keyboard:	For connection to an optional YK-01 or YK-10, 20 music keyboard. 20 pin male connector

POWER SUPPLY UNIT CAPACITY

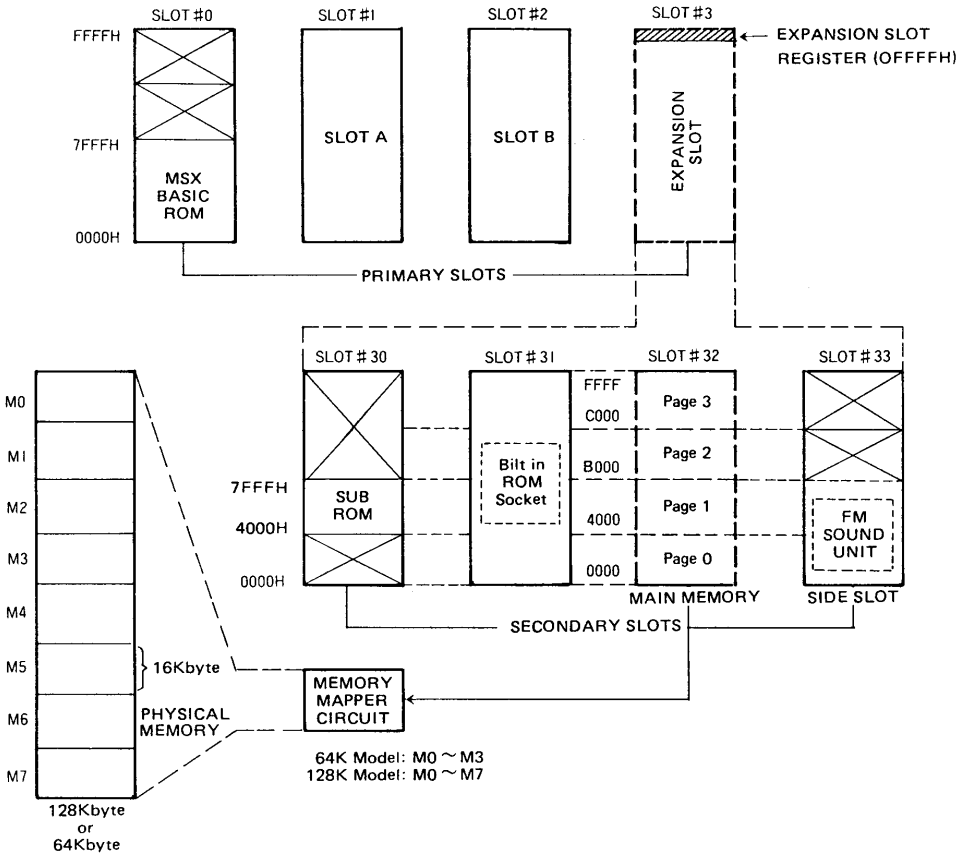
+5V ± 5% 2.0A
+12V ± 10% 0.3A
−12V ± 10% 0.16A

GENERAL SPECIFICATIONS

Line voltage:	CX-5MIIC 117V± 15%, 50/60Hz CX-5MIIE, F, A 220 ~ 240V, 50/60Hz CX-5MIIB, P 120V ± 10%, 50/60Hz 220V ± 10%, 50/60Hz Switchable
Power input:	10W 18W MAX
Measurement:	440(W) x 285(D) x 98(H)
Weight:	3.5 kg (about)
AC cable:	2,000 mm + 50 mm with AC plug (CX-5MIIC, F, A, B, P)

■ CX-5MII BRIEF DESCRIPTION

- **Memory map and slot area**



* Terminology: Primary slot . . . . . Slot which is enabled by slot select register with in MPS chips (I/O address 0A8H)
Secondary slot . . . Slot which is enabled by expansion slot register placed at 0FFFH (Memory address)
Page . . . . . Block of memory (maximum 16KB) in each slot. A slot is divided into 4 pages.

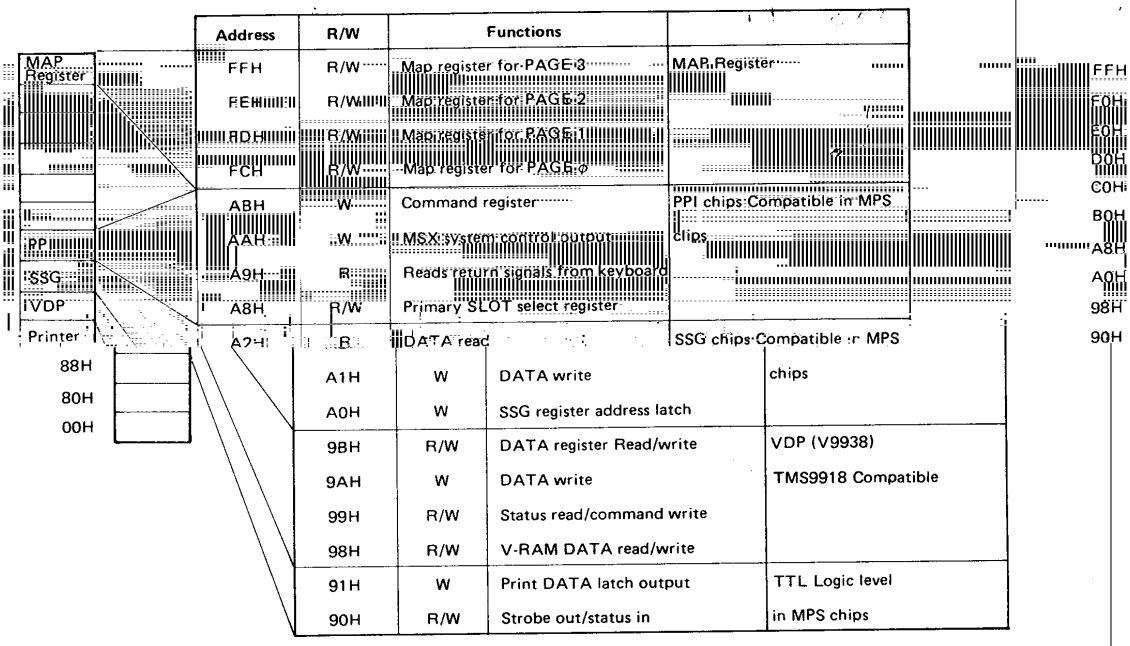
* Every select signal of each slot is output from MPS (100 pin LSI: S-3527)

MSX BASIC ROM	$\overline{\text{ROMCS}}$
SLOT A, SLOT B	$\overline{\text{SLT1}}$, $\overline{\text{SLT2}}$, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS12}}$
Extended BASIC ROM	$\overline{\text{SLT30}}$ (SUB ROM)
Built-in ROM socket	$\overline{\text{SLT31}}$, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS12}}$
Main memory area	MPX, $\overline{\text{WE}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS2}}$
Side slot	$\overline{\text{SLT33}}$, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS12}}$

* With the memory mapper circuit, the block by the unit of 16K bytes in the PHYSICAL MEMORY space can be mapped freely on each page of the MAIN MEMORY space.

area map

(Z80A) has a 256-bytes area as I/O ports. Under the MSX specification, the 256-bytes (00H ~ FFH) are
n the following way:



All I/O port addresses shown in the above I/O port area map are located within the 100-pin LSI (S-3527). The LSI encloses the μPD-8255A (PPI), YM2149 (SSG), and printer control circuit shown in the map. In addition, it has memory area and slot control functions.

MPS (S-3527) I/O ports register

^All the following MPS (S-3527) I/O ports provides the same control functions as the PPI (μPD-8255A) and SSG (YM2149):

I/O address A8H (PA0 ~ PA7): Slot select data register
A9H (PB0 ~ PB7): Keyboard scanning data input (return) port
AAH (PC0 ~ PC3): Keyboard scanning data output port
(PC4): Data recorder (cassette recorder) motor ON/OFF control bit
(PC5): Output FSK specification data to data recorder (cassette)
(PC6): CAPS LED control bit (on when "L")
(PC7): Emits beeping sound through 1 bit output

I/O address A0H ~ A2H
Internal SSG register number: 10H
(IOA0 ~ IOA5): Input port for general purpose. Input/output port (JOYSTICK 1, 2) data scanning.
(IOA6): Not used
(IOA7): Input port for data from data recorder (cassette).
Internal SSG regester number: 11H
(IOB0 ~ IOB3): JOYSTICK port scanning data output.
(IOB4): JOYSTICK 1 strobe signal output.
(IOB5): JOYSTICK 2 strobe signal output.
(IOB6): JOYSTICK 1 or 2 select signal
"L" . . . . JOYSTICK 1 selected
"H" . . . . JOYSTICK 2 selected

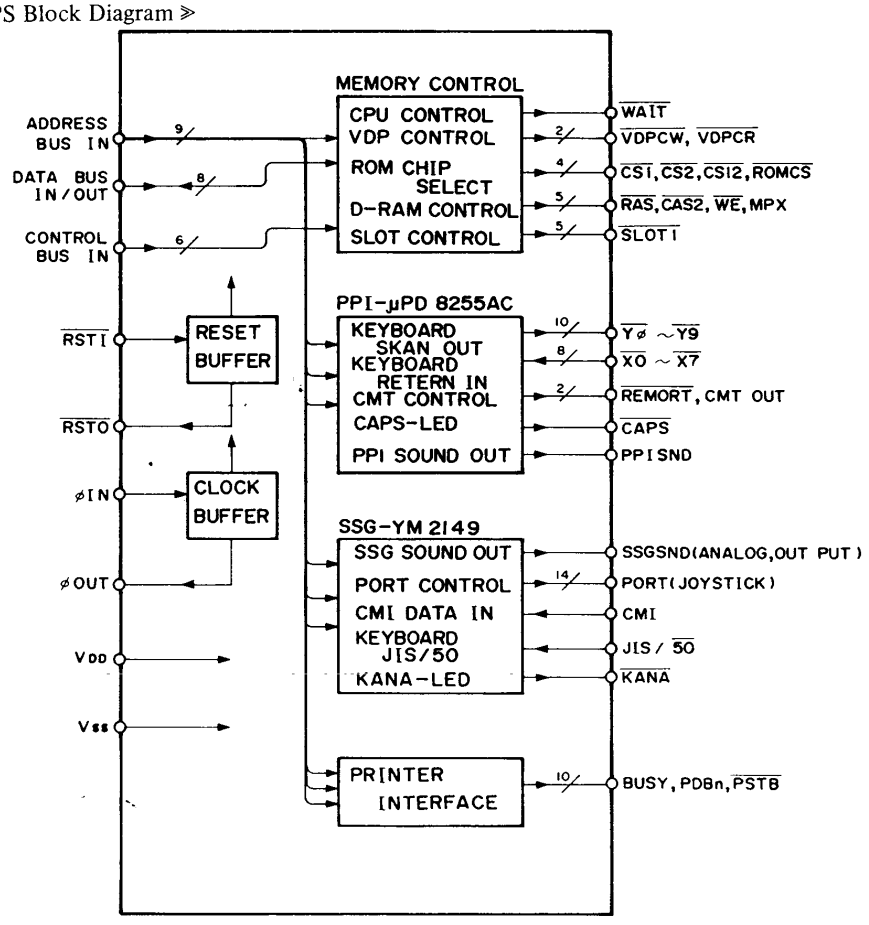
D-8255) and

- MPS (MSX Port Controller and Sound Generator): S-3527

The MPS (S-3527) is a 100-pin CMOS LSI specifically developed to support MSX. With a built-in PPI (μP SSG (YM-2149), the MPS provides the following system controller functions:

- Memory and slot area control
- ROM (MSX-BASIC ROM: 32K bytes) access
  $\overline{ROMCS}$
- RAM (D-RAM: 64K bytes) access
  $\overline{RAS}$, MPX, $\overline{WE}$, $\overline{CAS2}$
- Basic slot (# 1, # 2, # 3) control . . . Primary slot control
- Selection and control of expansion slots (# 00, # 01, # 02, # 03) . . . Secondary slot
- I/O area (I/O peripheral) control
- Printer contro
  $\overline{BUSY}$, PDBn, $\overline{PSTB}$
- VDP (video display processor) control
  $\overline{VDPCW}$, $\overline{VDPCR}$
- With a built-in PPI (μPD-8255) and SSG (YM-2149)
- 3-Channel 3-level voice and noise output
- Dual joystick (or general-purpose port) control
- Data recorder I/O control
- Keyboard control
- Insertion of 1 WAIT in the CPU M1 cycle
- RESET signal processing
- CPU clock (3.57954 MHz) input

≪ MPS Block Diagram ≫



* Removing MPS

age the pattern, as show in Figure A or fuse the solder with a special

damage the pattern

1 Cut the legs with a cutter, being careful not to dam
soldering iron as in Figure B.
2 After removing the MPS, desolder it with care not to

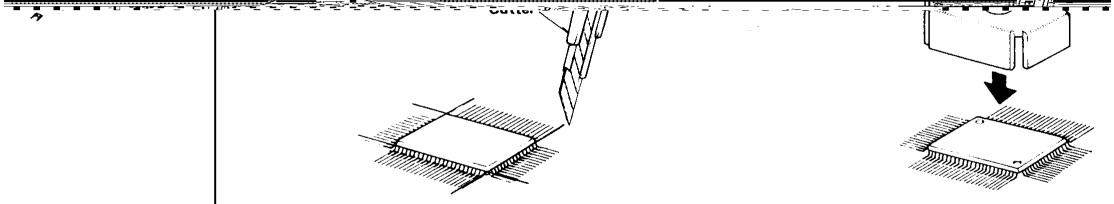


Fig. A

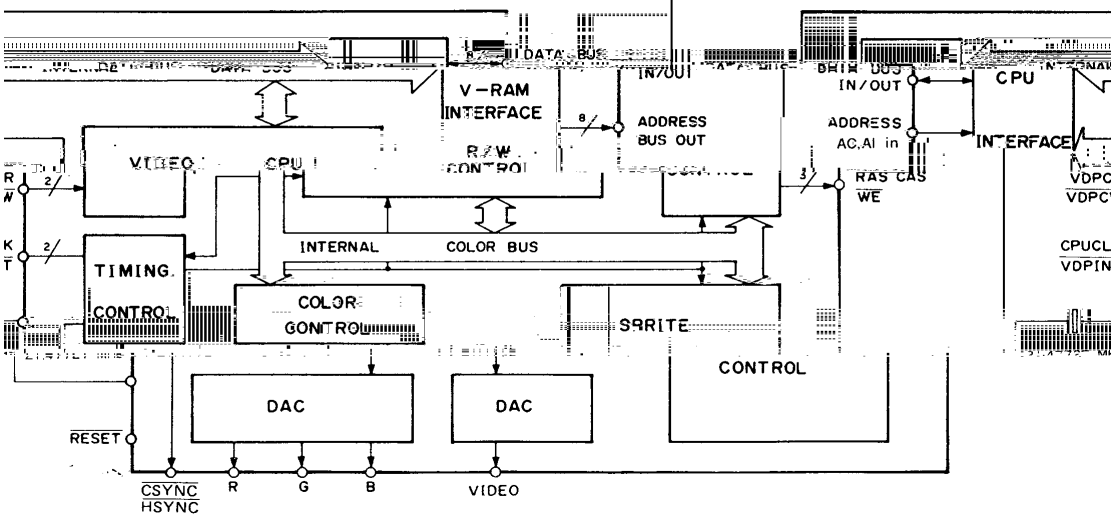
Fig. B

• VDP (Video Display Processor): V-9938

run on the MSX1

The VDP (V-9938) is a 64-pin MOS LSI developed for MSX2 concurrently with the MPS. The VDP is
specifications. It provides the following functions:
To provide software compatibility with the VDP (TMS9918A).
d from the linear
To generate linear RGB signals and composite video signals. Here, various video signals are produce
RGB signals without using the composite video signal.
To use 16K bytes as video RAM.
PU clock (3.579545 MHz). The clock generated by a quartz oscillator (21.47727 MHz) connected to pins
To supply a C

≪ VDP Block Diagram ≫



[redacted]

3FF4H		0	1	1	0	0	1	
3FF5H	0	0	1	1	0	1		MIDI standard UART DATA READ BUFFER
	0	1	0	1	0	1		MIDI standard UART DATA WRITE BUFFER
3FF6H	0	0	1	1	1	0		MIDI standard UART STATUS REGISTER
	0	1	0	1	1	0		MIDI standard UART COMMAND REGISTER
3FF7H				1	1	1		

■ MIDI RECEIVING AND TRANSMITTING DATA

The unit receives the following MIDI signals (when CALL MUSIC is functioning).

● MIDI receiving data

- **Channel message**

ignals

When the MIDI receiving channel is specified for each instrument, the unit receives the following MIDI s transmitted through the specified channel.

① **Key-OFF**

Status	1 0 0 0 n n n n (8 n H)	n = channel No.
Note No.	0 k k k k k k k	k = 0 (C-2) ~ 127 (G8)
Velocity	0 v v v v v v v	v : Neglected

② **Key-ON**

Status	1 0 0 1 n n n n (9 n H)	n = channel No.
Note No.	0 k k k k k k k	k = 0 (C-2) ~ 127 (G8)
Veleciry	0 v v v v v v v	v = 0 Key-OFF
		v = 1 ~ 127 Key-ON

③ **Control change**

Status	1 0 1 1 n n n n (B n H)	n = channel No.
Control No.	0 c c c c c c c	c = control No.
Control Value	0 v v v v v v v	

C = 5 Portamento time (SOLO mode only)
C = 7 Volume
C = 64 Sustain switch
C = 65 Portamento switch (SOLO mode only)
C = 125 All notes OFF

④ **Program change**

Status	1 1 0 0 n n n n (C n H)	n = channel No.
Program No.	0 p p p p p p p	p = program No. (0 ~ 47)

- **System real time message**

The unit receives the following system real time messages when the play clock is MIDI.

① **Timing clock**
Status 1 1 1 1 1 0 0 0 (F 8 H)

② **Start**
Status 1 1 1 1 1 0 1 0 (F A H)

③ **Continue start**
Status 1 1 1 1 1 0 1 1 (F B H)

④ **Stop**
Status 1 1 1 1 1 1 0 0 (F C H)

● MIDI transmitting data

The unit transmits the content played by the music keyboard and reproduction data through MIDI channel 1.

- **Channel voice message**

① **Key-OFF/Key-ON**

Status	1 0 0 1 0 0 0 0 (90 H)	
Note No.	0 k k k k k k k	k = 0 (C-2) ~ 127 (G8)
Velocity	0 v v v v v v v	v = 0 key-OFF
		v = 1 ~ 127 key-ON

- **System real time message**

The unit outputs the following system real time messages when the play clock is INTERNAL.

① **Timing clock**
Status 1 1 1 1 1 0 0 0 (F 8 H)

② **Start**
Status 1 1 1 1 1 0 1 0 (F A H)

③ **Stop**
Status 1 1 1 1 1 1 0 0 (F C H)

[8 Voices Polyphonic Synthesizer/Sequencer]

Model CX-5MIIMusic Function *MIDI Implementation Chart*

Date : 10, Apr, 1985

Version : 1.00

Function ...	Transmitted: Synthe.	Transmitted: Sequencer	Recognized: Solo	Recognized: Poly	Recognized: Seq	Recognized: Rh.	Remarks
Basic: Default	1	1	1	1	Same	×	* #2 ~ #4 off
Basic: Changed	1–16	1–16	1–16	1–16	as #1	×	
Mode: Default	3	3	3		×	×	
Mode: Messages	×	×	×		×	×	
Mode: Altered	**********	**********	×		*	×	
Note Number:	36–84	0–127	0–127			×	
Note Number: True voice	**********	**********	0–127		*	×	
Velocity: Note ON	× V=64	0 V=1–127	○			×	
Velocity: Note OFF	×	9nH V=0	×			×	
After Touch: Key's	×		×				
After Touch: Ch's	×		×				
Pitch Bender	×		×				
Control Change (5)	×		○	×		×	Portamento Speed
Control Change (7)	×		○	○		×	Volume
Control Change (64)	×		○	○		×	Sustain ON/OFF
Control Change (65)	×		○	×		×	Portamento ON/OFF
Prog Change:	×		○	0–47		×	
Prog Change: True #	**********	**********		0–47		×	
System Exclusive	×		×				
System Common: Song Pos	×		×				
System Common: Song Sel	×		×				
System Common: Tune	×		×				
System Real Time: Clock	○ (Internal Mode)		○ (MIDI Mode)				
System Real Time: Commands	○ (Internal Mode)	*	○ (MIDI Mode)				* Except FBH
Aux Mes-sages: Local ON/OFF	×		×			×	
Aux Mes-sages: All Notes OFF	○ (126, 127, 123)		○ (123)			×	
Aux Mes-sages: Active Sense	×		×			×	
Aux Mes-sages: Reset	×		×			×	

Notes:

In Split/Dual-Mode (of POLY Mode), MIDI Ch# of Inst#2 is same as Inst#1'S

In order to clear all notes, we send [All notes OFF (126, 127, 123)]

Mode 1 : OMNI ON, POLY Mode 2 : OMNI ON, MONO ○ : Yes

Mode 3 : OMNI OFF, POLY Mode 4 : OMNI OFF, MONO × : No

OT A AND SLOT B ASSIGNMENT

Pin No.	Pin Name	I/O	Description
1	$\overline{CS1}$	O	Select Signal for ROM 4000H-7FFFH
2	$\overline{CS2}$	O	Select Signal for ROM 8000H-BFFFH
3	$\overline{CS1,2}$	O	Select Signal for ROM 4000H-BFFFH
4	$\overline{SLTSL}$	O	Slot Select Signal
5	N/C	–	Inhibited to use
6	$\overline{RFSH}$	O	Dinamic RAM refresh signal
7	$\overline{EXT\ WAIT}$	I	WAIT request, open collector signal
8	$\overline{EXT\ INT}$	I	Maskable interrupt request, open collector signal
9	$\overline{M1}$	O	M1 signal from CPU
10	$\overline{BUSDIR}$	I	Direction Control for external Bus Buffer
11	$\overline{IORQ}$	O	I/O request from CPU
12	$\overline{MERQ}$	O	Internal memory request from CPU
13	$\overline{WR}$	O	Write request from CPU
14	$\overline{RD}$	O	Road request from CPU
15	$\overline{RESET}$	O	System Preset signal
16	N/C	–	Inhibited to use
17	A9	O	Address Bus signal
18	A15	O	
19	A11	O	
20	A10	O	
21	A7	O	
22	A6	O	
23	A12	O	
24	A8	O	
25	A14	O	
26	A13	O	
27	A1	O	
28	A0	O	
29	A3	O	
30	A2	O	
31	A5	O	
32	A4	O	
33	D1	I/O	Data Bus signal
34	D0	I/O	
35	D3	I/O	
36	D2	I/O	
37	D5	I/O	
38	D4	I/O	
39	D7	I/O	
40	D6	I/O	
41	GND	–	Ground
42	CLOCK	O	System Clock 3.579545MHz
43	GND	–	Ground
44	SW1	–	System protection
45	+5	–	Power Supply +5V
46	SW2	–	System protection (Note: SW1 and SW2 is in connection when Cartridge is inserted.)
47	+5	–	Power Supply +5V
48	+12	–	Power Supply +12V
49	SOUND IN	I	Sound input line (−5dbm) mixed with PSG sound and output
50	−12	–	Power Supply −12V

- SIDE SLOT assignment

Pin No.	Pin Name	I/O	Description
1	SOUND OUT	O	Mixing Sound out of SSG, PP1
2	GND	–	Ground
3	GND	–	Ground
4	NC	–	Non connect
5	NC	–	
6	NC	–	
7	VIDEO	O	Video Out
8	NC	–	Non connect
9	NC	–	
10	NC	–	
11 ~ 60			Exactly same as regular slot

f PROCEDURES

ith Repair:

: or cover.
: center of the bottom case.
M cartridge cover. If a ROM cartridge has been installed, remove it also.
tery cover, remove the battery. (only MSX_2 Version)

ed by pushing it at claws with a standard screwdriver as shown in Figure A. There are four claws.
e.
our claws, detach the top case by lifting it a little on the rear side. The top case is fixed on the
shown in Figure B. Never use undue force to release it.

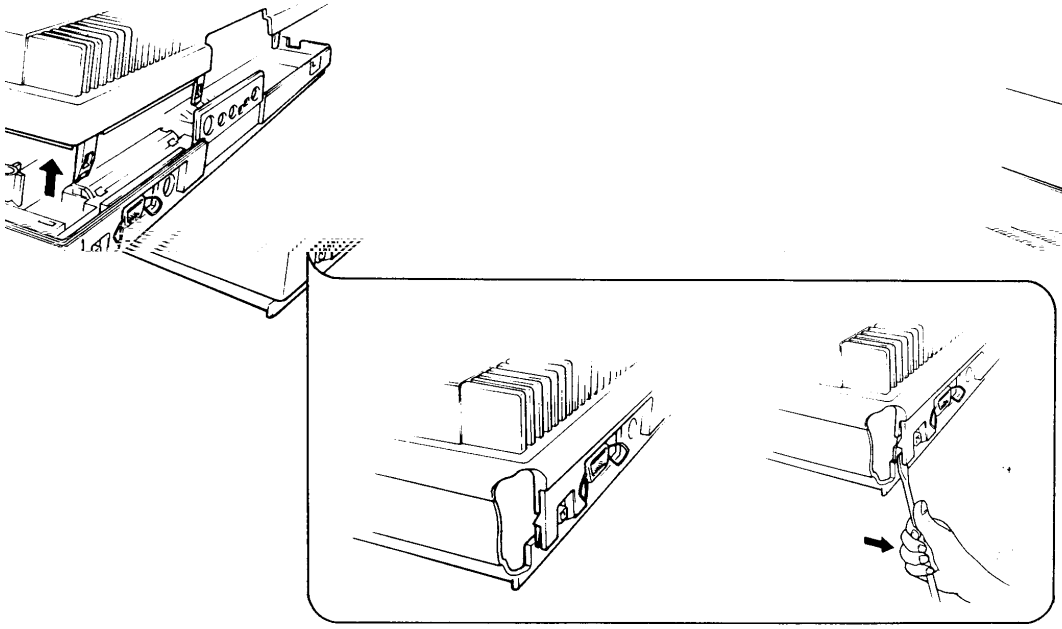


Fig. A

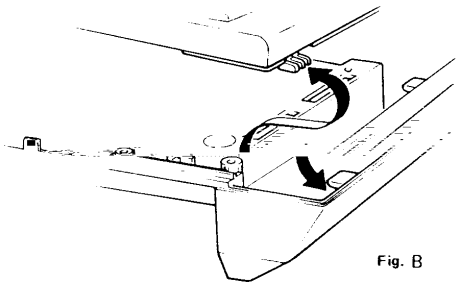


Fig. B

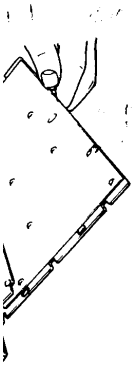
■ DISASSEMBL

- *Before Proceeding w*

1 Detach the side slot unit
2 Remove the screw in the
3 Remove the built-in RO
4 Uncover the backup bat

1) Top Case Removal

1 The top case can be lift
Release them one by on
2 After releasing all the f
front side at the claw as



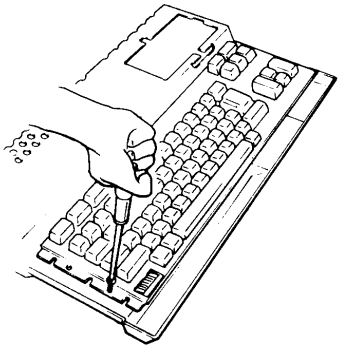
tall them.

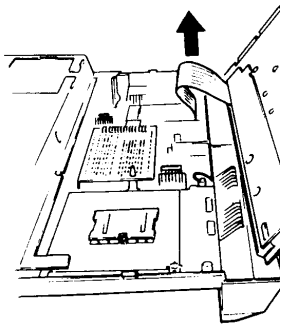
(power switch and power

if case, lift the CPU board on the

2) Keyboard Unit Removal

1 Remove four screws on both sides (four in total) of the keyboard unit.
2 Lift off the keyboard unit, slowly removing the flat cable from the CPU circuit board.
3 Remove Upper shield (only CX-5MIIU, G)





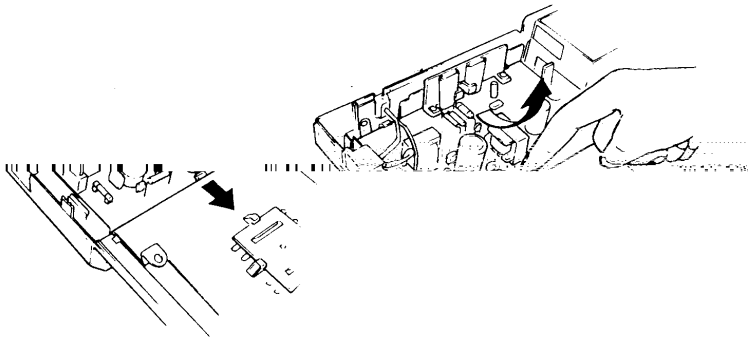
- *Board and Unit Removal Procedures*

Remove the boards and units in the following sequence. Reverse the removal procedures to reins

Step 1) Power supply unit removal
Step 2) Video module unit removal
Step 3) Side slot earth plate removal
Step 4) Main CPU board removal
Step 5) Bottom shield removal

3) Power Supply Unit Removal

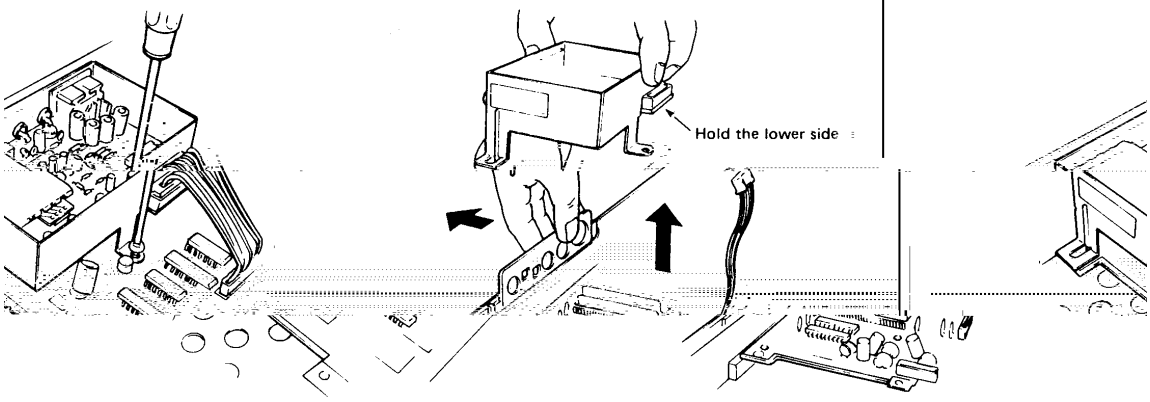
1 Pull out the power connector attached to the power supply unit. Next, disconnect the AC inlet
cable). Then, pull out the connector (bundled wires) from the CPU circuit board.
2 Remove four screws. Next, pulling forward the stopper claw extending from the bottor
front side. Then, remove the power supply unit by pulling it forward as a whole.



Removal
from the CPU circuit board.

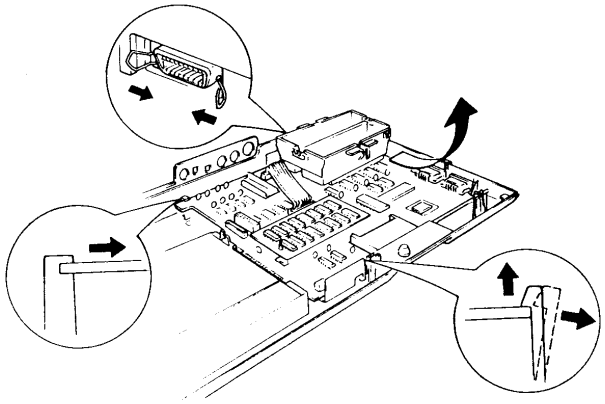
inward a little, lift off the video module unit.
t has legs as shown. Be careful not to damage them during removal.)
ctor to the video module unit, insert it while holding the lower side of the circuit board as it is

4) Video Module Unit
1 Pull out the connector
2 Remove two screws.
3 Pushing the rear panel
(The video module uni
* *In attaching the conne*
easily cracked.



5) CPU Circuit Board Removal

1 Remove seven screws securing the CPU circuit board in position.
2 Remove the side slot earth plate.
3 Release the two stopper claws extending from the bottom case by lifting the board a little on the front side. Then, remove the CPU circuit board by pulling it forward. Note that the in CPU circuit board is also secured in position by two stopper claws from the bottom case. The printer connector stoppers may be secured with a rubber band to facilitate servicing.



ounding plate

* The video RAM circuit board and the main RAM circuit board are screwed to the bottom case by a gr each. Follow the steps below to remove these boards.

ase the board

6) Video RAM Circuit Board Removal

1 Remove one screw securing the video modulation unit, or remove the video modulation unit. Next, rele stopper claws.
2 Detach the video RAM circuit board from the CPU circuit board connector.

d connector.

7) Main RAM Circuit Board Removal

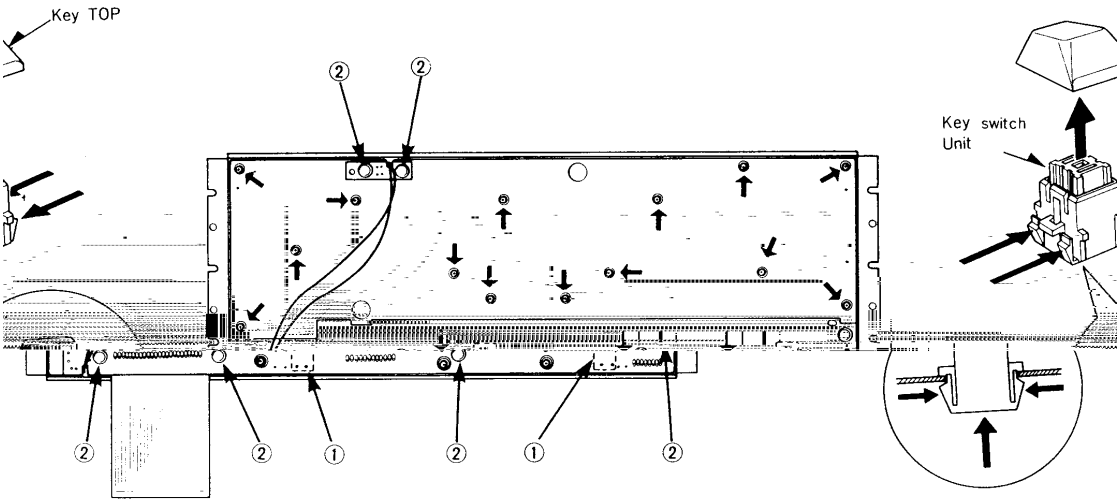
1 Remove one screw securing the power supply unit, or remove the power supply unit.
2 Remove the side slot earth plate.
3 Next, release the board stopper claws and detach the main RAM circuit board from the CPU circuit boar

8) Overhauling Keyboard Unit

1 Desolder S64, S65, D2, and D5 (CAPS and CODE key switches and D4, D5) on the sub-circuit board fr

ver LED. Extract

2 Raise the sub-circuit board by removing the six plastic pins securing the sub-circuit board and the pov the CN2 and CN3 flat cables at this time ② .
3 Remove the switch frame by unscrewing 17 special screws.
4 Pull out the keytops slowly as shown.
5 The key switch unit can be removed by holding it on the left and right claws and pushing them inward.



■ ADJUSTMENTS

Adjustment	Equipment required	Measure at	Adjust	Readings
+5V supply voltage	DVM (Digital voltmeter)	Pin #4 and 7 of connector CN2, CPU board	VR101 power supply	+5V ± 0.25V
Clock frequency	Frequency counter	Pin #6 of Z80A CPU		3.579545MHz ± 500Hz

Notes) Check AC line voltage to insure that it is specification voltage ± 10%.
The adjustment for +5V supply voltage should be made while the circuitry of the CX-5MII is connected.

- Measurement

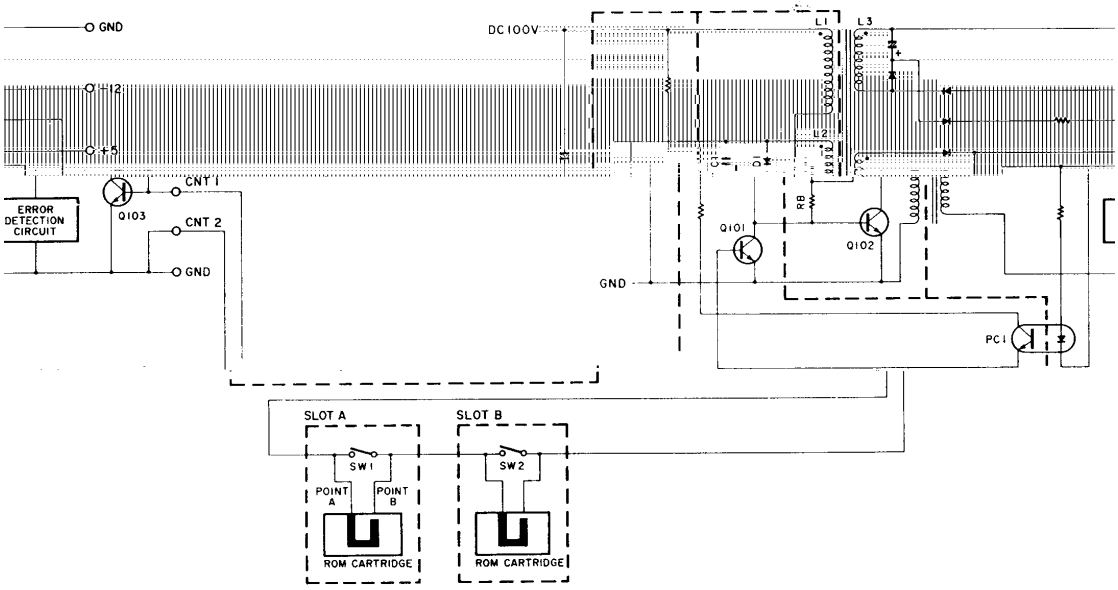
Item	
Conditions	• Connect power circuit to CPU board. • Apply no load to each slot (game cartridge, etc.) of CPU board. • Don't connect peripheral equipments (printer, JOYSTICK, etc.).
Voltage	+5V ± 5%
Voltage to be confirmed	• −12V (1 pin) & GND: −12V ± 12.5% • +12V (2, 3 pin) & GND: +12V ± 12.5%

• Adjust VR101 so that the above listed voltages are obtained at each voltage output pin with each unit connected. Also, confirm that the output voltage is within the tolerance range even when the power voltage is 220 to 240V or 117V.

• Check to make sure that each output voltage is within the cartridge protect voltage when the micro switch of the upper slot is turned OFF (pressed) or the 9 pin circuit of CN102 is opened.

Circuit name	Voltage	Tolerance range	Cartridge protect voltage
−5V	+5V	± 5V	Within 1V
+12V	+ 12V	± 12.5V	Within 2V
−12V	−12V	± 12.5V	Wihtin 2V

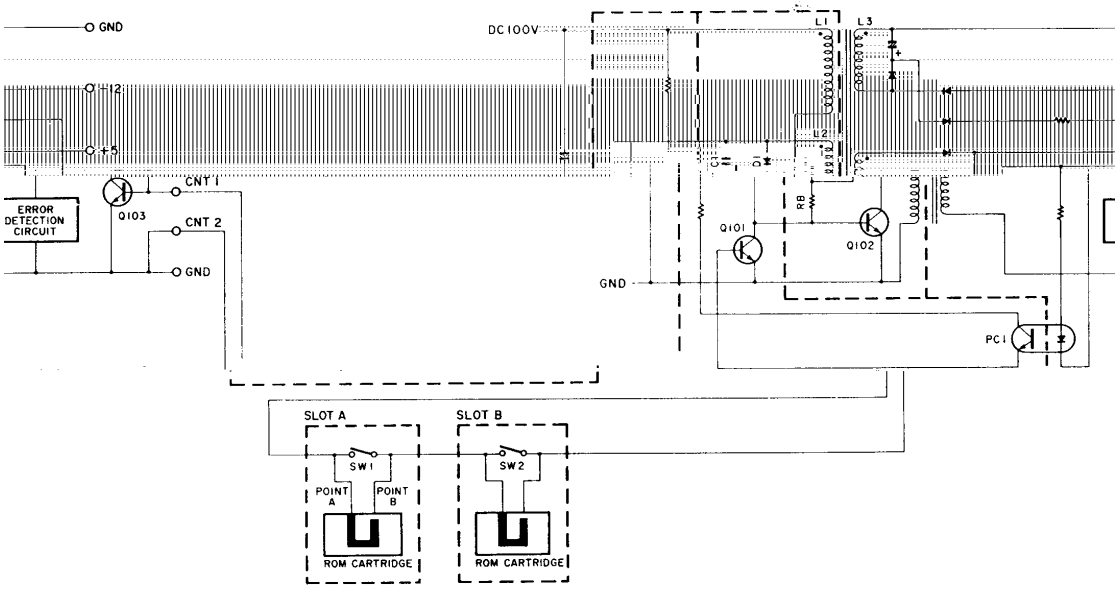
■ OPERATION OF POWER SUPPLY CIRCUIT



The following is the destination and operation of the circuit.

1. In D1, C1 and RB are the base drive circuits, and the base current of Q102 is determined by RB.
2. Q101 operates as a voltage controller and cartridge protector.
3. The photocoupler (PC1) feeds the voltage fluctuation of +5V back to the control circuit through the error detection circuit at all times. The control circuit controls output, based on the information fed back, by increasing and decreasing the base current of Q101 changing the oscillating frequency of Q102.
4. SW1, SW2 connected to Q103 in the cartridge protector circuit is ON at all times.
5. When Q103 is ON and the ROM cartridge is set in the slot-A erroneously, SW1 is turned OFF.
   Next, Q103 is turned ON, and the current flowing in the photocoupler (PC1) increases.
   Then, the photocoupler (PC1) on the control circuit is turned ON to turn ON Q101.
   The oscillating frequency of Q102 increases, the energy stored in L1 decreases, and output voltage lowers. When the ROM cartridge is properly set afterwards, A and B points in Fig. A are short-circuited, and voltage increases again.

■ OPERATION OF POWER SUPPLY CIRCUIT



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■ LSI DATA TABLE

- CPU (LH0080A)

PIN NO.	PIN NAME	I/O	ACTIVE	FUNCTION
1～5	A11, 12, 13, 14, 15	O		Address bus
6	ϕ	I		CPU clock input (3.579545MHz)
7～10	CD4, 3, 5, 6	I/O		Data bus
11	VDD	I		Voltage Supply +5V
12～15	CD2, 7, 0, 1	I/O		Data bus
16	$\overline{INT}$	I	L	Mask-able interrupt input pin: Mode 1 is used for interrupt of MSX-BASIC which is input by taking the logic OR of the VDP interrupt output (every 1/60s) and the cartridge interrupt input ($\overline{EXTINT}$).
17	$\overline{NMI}$			Non-connect
18	$\overline{HALT}$			Non-connect
19	$\overline{MREQ}$	O	L	Active when the effective address for memory access is on the address bus.
20	$\overline{IORQ}$	O	L	Active when the effective address for the input/output port access is on the address bus (also active when in INT or ACK cycle)
21	$\overline{RD}$	O	L	Active during the period when the CPU can receive data from the memory and input/output port.
22	$\overline{WR}$	O	L	Active when the CPU sends data to be stored in the memory and input/output port to the data bus.
23	$\overline{BUSAK}$			Pull up (+5V)
24	$\overline{WAIT}$	I	L	CPU remains in the wait state as long as this signal is active "L". (No refresh signal is generated when in the WAIT state.)
25	$\overline{BUSRQ}$			Non-connect
26	$\overline{RESET}$	I	L	The program counter becomes "0" at the $\overline{RESET}$ input and the CPU is initialized.
27	$\overline{M1}$	O	L	One "L" pulse is output at each instruction fetch cycle (also active when in the INT or ACK cycle)
28	$\overline{RFSH}$	O	L	Active when the low order 7 bit refresh address for D-RAM is on the address bus
29	Vss	I		Ground
30～40	A0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	O		Address bus

- MPS (S3527)

PIN NO.	PIN NAME	I/O	ACTIVE	FUNCTION
1	CMI	I		Read signal input from cassette tape
2	CMO	O		Write output to cassette tape
3	REM	O		Cassette control signal output (motor ON/OFF control)
4	PRISND	O		Software-controlled sound output
5	SSGSND	O		SSG anlog sound output
6	Vss			0V SSG ground
7	$\overline{VDPCW}$	O		VDP (Video Display Processor) write timing signal output
8	$\overline{VDPCR}$	O		VDP read timing signal output
9	$\overline{RSEL}$	I	*	Slot expansion address input
10～18	AB15～AB0	I		Z80A CPU address bus input (9 bits) (AB15, AB14, AB7, AB6, AB5, AB4, AB3, AB1, AB0)
19～26	DB7～DB0	I/O		Z80A CPU data bus I/O (8 bit)
27	$\overline{SLT03/33}$	O		Expanded slot 03 select signal
28	$\overline{SLT01/31}$	O		Expanded slot 01 select signal
29	ϕOUT	O		Z80A CPU clock output
30	ϕIN	I		Clock input (This signal is used via a buffer for clock input to other than the Z80A).
31	Vss			0V ground
32	$\overline{RST0}$	O		Slot expansion initialization signal input
33	$\overline{RST}$	I	*	Slot expansion initialization signal input (RESET signal input)
34	$\overline{M1}$	I		Z80A CPU M1 input
35	$\overline{RFSH}$	I		Z80A CPU RFSH input
36	$\overline{MREQ}$	I		Z80A CPU input
37	$\overline{IORQ}$	I		Z80A CPU IORQ input
38	$\overline{RD}$	I		Z80A CPU RD input
39	$\overline{WR}$	I		Z80A CPU WR input
40	VDD			+5V power supply

45	$\overline{CAS3}$	O		D-RAM CAS signal output (CAS3: SLOT #0 C000 ~ FFFF)
46	$\overline{CAS2/E}$	O		D-RAM CAS signal output (CAS2/E: SLOT #32 0000 ~ FFFF)
47	$\overline{WE}$	O		D-RAM write enable signal output
48	FWD 1	I	*	JOYSTICK FWD 1 signal or general-purpose port input
49	BACK 1	I	*	JOYSTICK BACK 1 signal or general-purpose port input
50	LEFT 1	I	*	JOYSTICK LEFT 1 signal or general-purpose port input
51	RIGHT 1	I	*	JOYSTICK RIGHT 1 signal or general-purpose port input
52	TRGA 1	I/O	*/△	JOYSTICK TRGA 1 signal or general-purpose port output (I/O by wired logic)
53	TRGB 1	I/O	*/△	JOYSTICK TRGB 1 signal or general-purpose port output (I/O by wired logic)
54	STB 1	O		General-purpose port output
55	FWD 2	I	*	JOYSTICK FWD 2 signal or general-purpose port input
56	BACK 2	I	*	JOYSTICK BACK 2 signal or general-purpose port input
57	LEFT 2	I	*	JOYSTICK LEFT 2 signal or general-purpose port input
58	RIGHT 2	I	*	JOYSTICK RIGHT 2 signal or general-purpose port input
59	TRGA 2	I/O	*/△	JOYSTICK TRGA 2 signal or general-purpose port output (I/O by wired logic)
60	TRGB 2	I/O	*/△	JOYSTICK TRGB 2 signal or general-purpose port output (I/O by wired logic)
61	$\overline{STB\ 2}$	O		General-purpose port output
62	$\overline{Y10/SK}$		*/△	Not used (Keyboard scanning signal output (1 bit))
63	JIS/50	I	*	Keyboard layout control input
64	$\overline{CAPS}$	O	△	CAPS LED control signal output (Direct lighting of LED possible)
65	$\overline{CODE}$	O	△	CODE LED control signal output (Direct lighting of LED possible)
66 ~ 73	$\overline{X0} \sim \overline{X7}$	I	*	Keyboard return signal input (8 bits) (X6 serves as function select input on a reset.)
74 ~ 83	$\overline{Y0} \sim \overline{Y9}$	O	△	Keyboard scanning signal output (10 bits)
84	$\overline{CS1}$	O		ROM select signal output (4000 ~ 7FFF)
85	$\overline{CS2}$	O		ROM select signal output (8000 ~ BFFF)
86	$\overline{CS12}$	O		ROM select signal output (4000 ~ BFFF)
87	$\overline{SLT1}$	O		Slot select signal output (SLOT #1)
88	$\overline{SLT2}$	O		Slot select signal output (SLOT #2)
89	$\overline{SLT3/30}$	O		Slot select signal output (SLOT #3)
90	VDD			+5V power supply
91	BUSY	I	*	Printer status input
92 ~ 99	PD87 ~ PD80	O		Print data output (8 bits)
100	$\overline{PSTB}$	O		Printer strobe output

Note) * With pullup resistor (≃22K) △ Open Drain (Pull Down) OUTPUT

- VDP (V9938)

PIN NO.	PIN NAME	I/O	FUNCTION
1	GND		Ground
2	$\overline{\text{DHCLK}}$	O	Not used
3	$\overline{\text{DLCKL}}$	I/O	
4	$\overline{\text{VDS}}$	O	Not used
5	HSYNC	I/O	High level (high to middle): output, low level (middle to low): input High: Non-HSYNC timing or color burst timing Middle: HSYNC timing or color burst timing Low: HSYNC input
6	CSYNC	I/O	High level: composite SYNC output, low level: VSYNC input
7	BLEO	O	Not used
8	CPU CLK	O	1/6 X'TAL frequency output
9	$\overline{\text{RESET}}$	I	MSX-VIDEO circuit initialization
10	$\overline{\text{YS}}$	O	Not used
11	CBDR	O	Not used
12 ~ 19	C7 ~ C0	I/O	Not used
20	GND		DAC ground
21	VIDEO	O	Not used (Composite video signal output)
22	G	O	Linear RGB signal output
23	R	O	Linear RGB signal output
24	B	O	Linear RGB signal output
25	$\overline{\text{INT}}$	O	CPU interrupt request signal output (low: Interrupt-request)
26	$\overline{\text{LPS}}$	I	Not used
27	$\overline{\text{LPD}}$	I	Not used
28	MODE 1	I	CPU interface mode select signal
29	MODE 0	I	CPU interface mode select signal
30	$\overline{\text{CSW}}$	I	CPU-VDP write strobe
31	$\overline{\text{CSR}}$	I	CPU-VDP read strobe
32	CD7	I/O	CPU-data bus
33	VBB	O	Circuit board voltage
34 ~ 40	CD0 ~ CD6	I/O	CPU data bus
41 ~ 48	RD0 ~ RD7	I/O	VRAM data bus
49 ~ 56	AD0 ~ AD7	O	VRAM address bus
57	R/W	O	VRAM write strobe
58	Vcc		+5V power supply
59	$\overline{\text{CASX}}$	O	Not used
60	$\overline{\text{CAS1}}$	O	Not used
61	$\overline{\text{CAS0}}$	O	VRAM column address strobe
62	$\overline{\text{RAS}}$	O	VRAM low address strobe
63	XTAL 1	I	X'TAL connection (Externally oscillated clock is input to this pin.)
64	XTAL 2	I	X'TAL connection (Externally oscillated clock is input to this pin.)

Note) * With pullup resistor (≃ 22k) △ Open Drain (Pull Down) OUTPUT

- 16Kbit x 4 DRAM (MB81416-12)

PIN NO.	PIN NAME	I/O	ACTIVE	FUNCTION
1	$\overline{\text{OE}}$	I		Output enable
2, 3	DQ1, DQ2	I/O		Data output
4	$\overline{\text{WE}}$	I		Write enable, write mode at active "L"
5	$\overline{\text{RAS}}$	I		Lower address strobe
6 ~ 8	A6, 5, 4	I		Address input
9	VDD			Voltage Supply +5V
10 ~ 14	A7, 3, 2, 1, 0	I		Address input
15	DQ3	I/O		Data output
16	$\overline{\text{CAS}}$	I		Column address strobe
17	DQ4	I/O		Data output
18	Vss			Ground
				Note) MB81416 is an N channel MOS RAM consisting of 16384 word x 4 bit. $\overline{\text{RAS}}$ only refresh type, write cycle (early write) type.

• 64Kbit DRAM (MB8264)

PIN NO.	PIN NAME	I/O	ACTIVE	FUNCTION
1	N.C			Non Connect
2	D in	I		Data input
3	WE	I	L	Write enable, write mode to D-RAM at active "L"
4	RAS	I	L	Lower address strobe
5~7	A0, 2, 1	I		Address bus input
8	Vcc			+5V
9~13	A7, 5, 4, 3, 6	I		Address bus input
14	Dout	O		Data output
15	CAS	I	L	Column address strobe
16	Vss			Ground

• EAO (YM3012)

PIN NO.	PIN NAME	I/O	FUNCTION
1	VDD	—	+5V power
2	CLOCK	I	Timing clock for synchronizing with OPE
3	GND	—	
4	DATA	I	Tone sirial data
5	SAM2	I	Sampling data (for LR separator)
6	SAM1	I	Sampling data (for LR separator)
7	ICL	I	Initial clear
8	GND	—	Ground for analog
9	CH1	O	1CH (L-CH) analog signal
10	CH2	O	2CH (R-CH) analog signal
11	COM	O	Offset control
12	To BUF	O	Offset control
13	Mid-point	O	Offset control
14	BIAS compensation	O	Offset control
15	BIAS	O	Offset control
16	GND	—	

- MKS (YM2148)

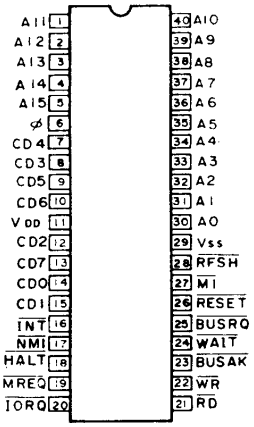
PIN NO.	PIN NAME	I/O	FUNCTION	REMARKS
1	Vss	–	Ground	
2 ~ 4	A_0 ~ A_2	I	Selection signal for internal registers	
5	$\overline{CS}$	I	Chip select	
6	$\overline{WT}$	I	Write request for data from CPU	
7	$\overline{RD}$	I	Read request for data from CPU	
8	$\overline{OPM}$	O	Address decode out to OPM	Output when A_0 to A_1 address input is 0 or 1.
9 ~ 16	ST_0 ~ ST_7	O	Used as strobe output to keyboard	Latch output ports in 2nd address
17	VDD	–	+5V power	
18	RXD	I	MIDI serial data	
19 ~ 26	SD_0 ~ SD_7	I	Data input port	Data input ports to 2nd address
27	TXD	O	MIDI serial data	
28 ~ 35	D_0 ~ D_7	I/O	3-state data bus I/O ports	
36	$\overline{VR}$	I	VECTOR ADDRESS REQUEST	Used for Z-80 MODE 2, IRQ Maskable
37	IRQ	O	Interrupt request generated when receiving and transmitting MIDI signal	
38	$\overline{IC}$	I	"L" reset data IRQ "H", $\overline{OPM}$ "H"	$\overline{ST0}$ ~ $\overline{ST7}$ "H", D0 ~ D7 "Hi impedance"
39	ϕA	I	Clock for MIDI baud rate generation	
40	ϕ	I	CPU Master clock for synchronizing with CPU	

- OPM (YM2151)

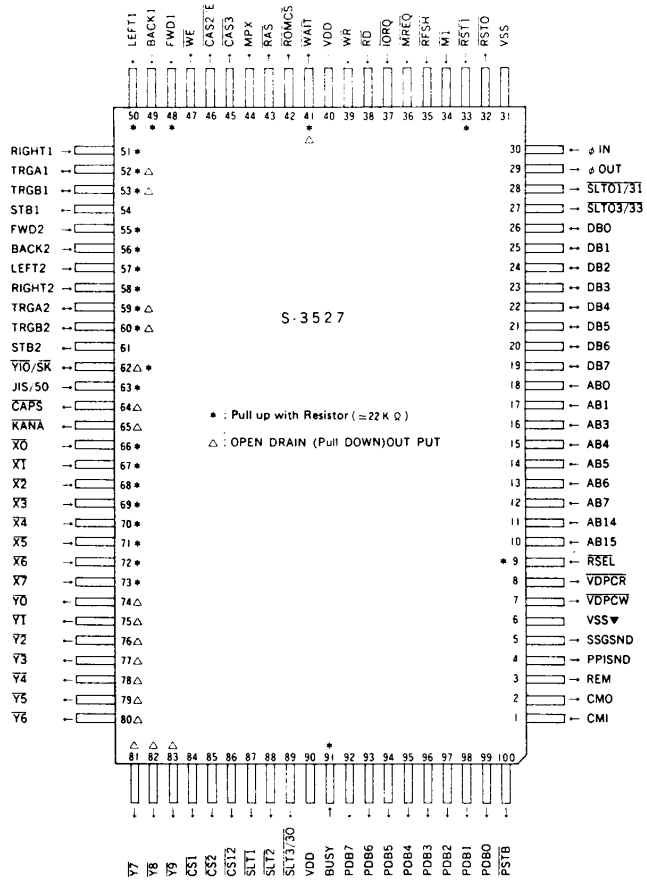
PIN NO.	PIN NAME	I/O	FUNCTION	REMARKS
1	$\overline{Vss}$	–	Ground	
2	$\overline{IRQ}$		Interrupt request output port	
3	$\overline{IC}$	I	"L" reset	
4	A_0	I	Selection signal for internal register	
5	$\overline{WT}$	I	Write request for data from CPU	
6	$\overline{RD}$	I	Read request for data from CPU	
7	$\overline{CS}$	I	Chip select	
8			Not used	
9	$\overline{CT1}$	O	Signal for switching voice synchesis filter characteristics	
10	D_0	I/O	3-state data bus I/O port	
11	Vss	–	Ground	
12 ~ 18	D_1 ~ D_7	I/O	3-state data bus I/O ports	
19	SH1	O	Signal for separating L and R	
20	SH2	O		
21	S_0	O	Serial data for sound source (L, R)	
22	VDD	–	+5V power	
23	ϕ1	O	Clock for DAC synchronization	
24	ϕ	I	CPU Master clock for synchronizing with CPU	

■ LSI PIN CONFIGURATION

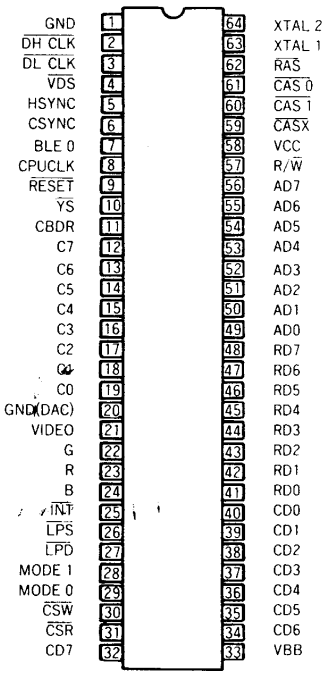
Z—80A (CPU)



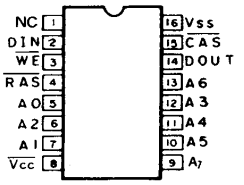
S3527 (MPS)



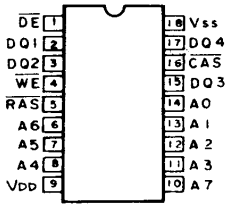
V9938 (VDP)



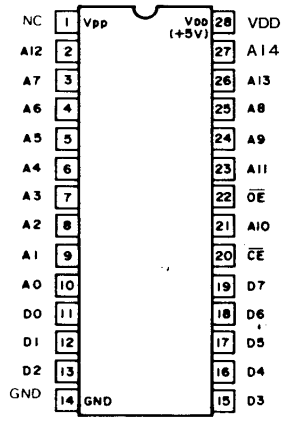
MB8264 (RAM)



MB81416-12 (RAM)

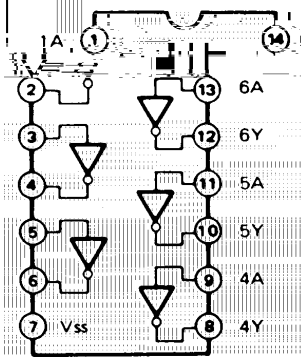


256K bit (EP-ROM)

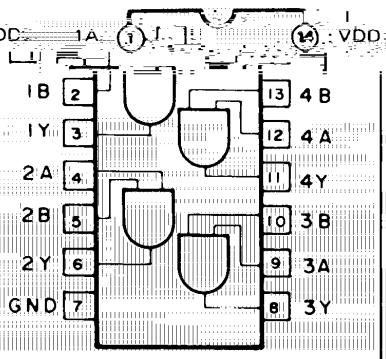


■ IC DIAGRAM

• HD74S04
Quad 2-Input NOR

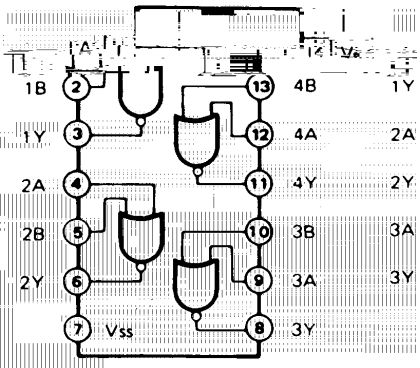


• HD74LS04
Hex Inverters

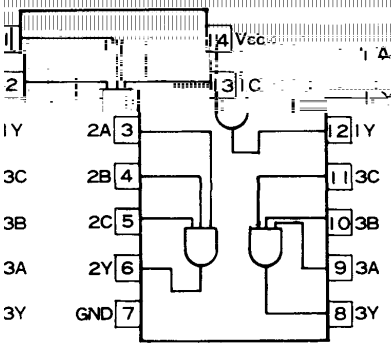


• 74LS08

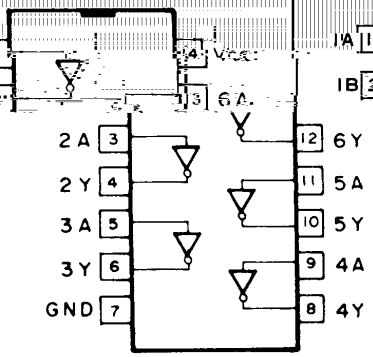
• HD74LS02
Quad 2-Input NAND



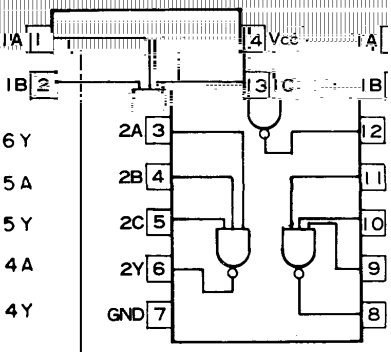
• HD74LS11
Tri 3-Input AND



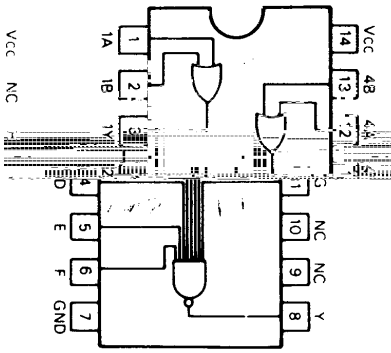
• 74LS14
Hex Schmitt
Trigger Inverters



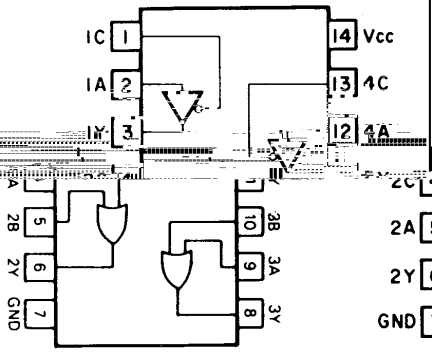
• 74LS10
Tri 3 Input NAND



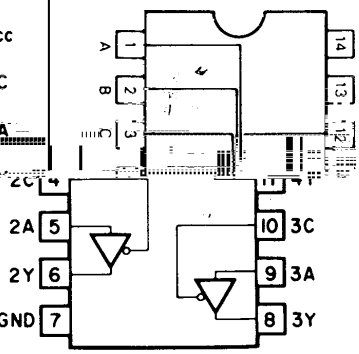
• 74LS32
Quad 2-Input OR

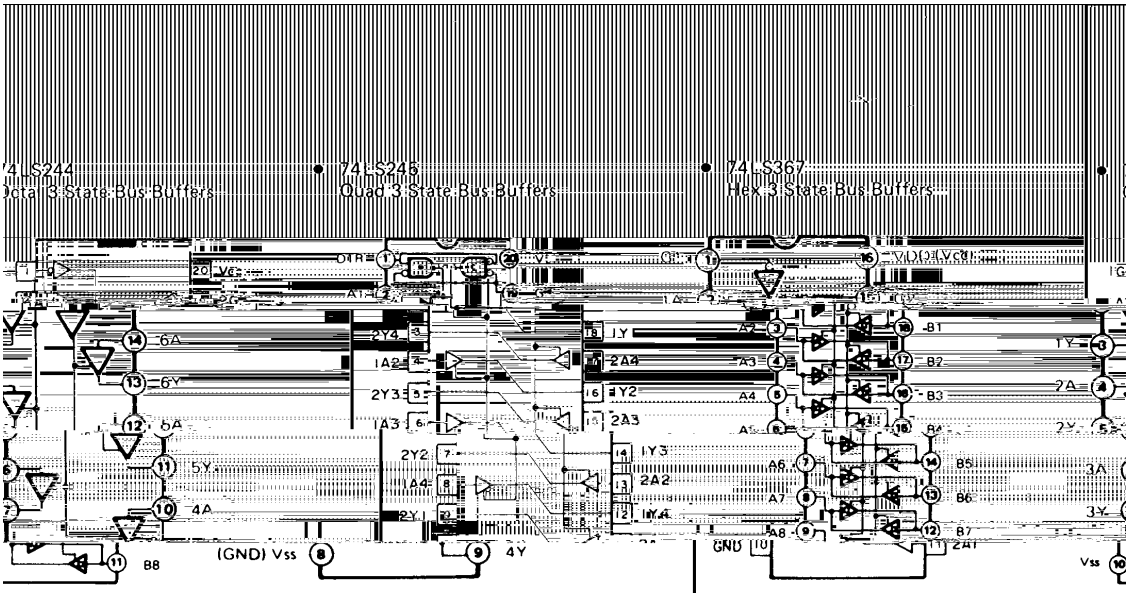


• 74LS125
Quad 3 State Bus Buffers

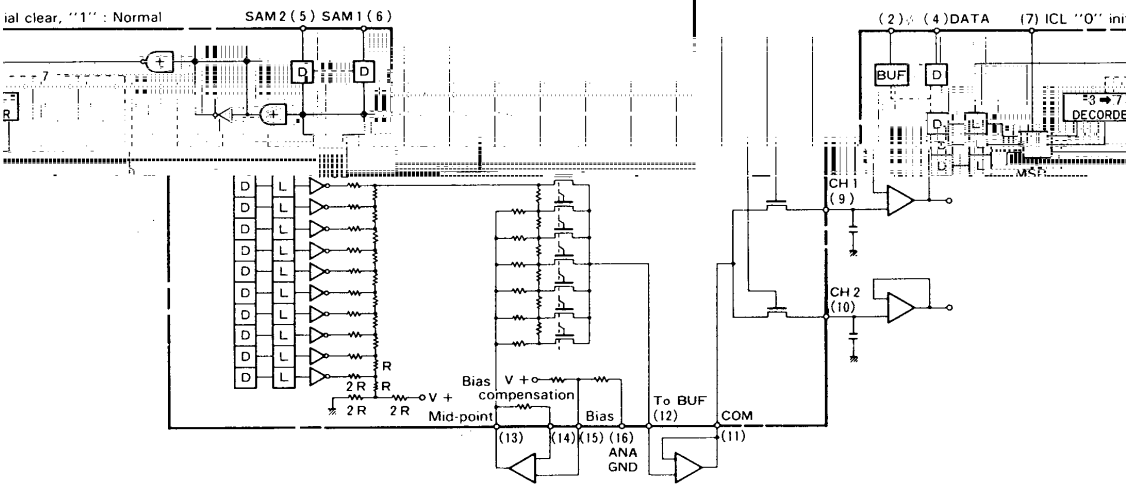


• 74LS30
8 Input NAND

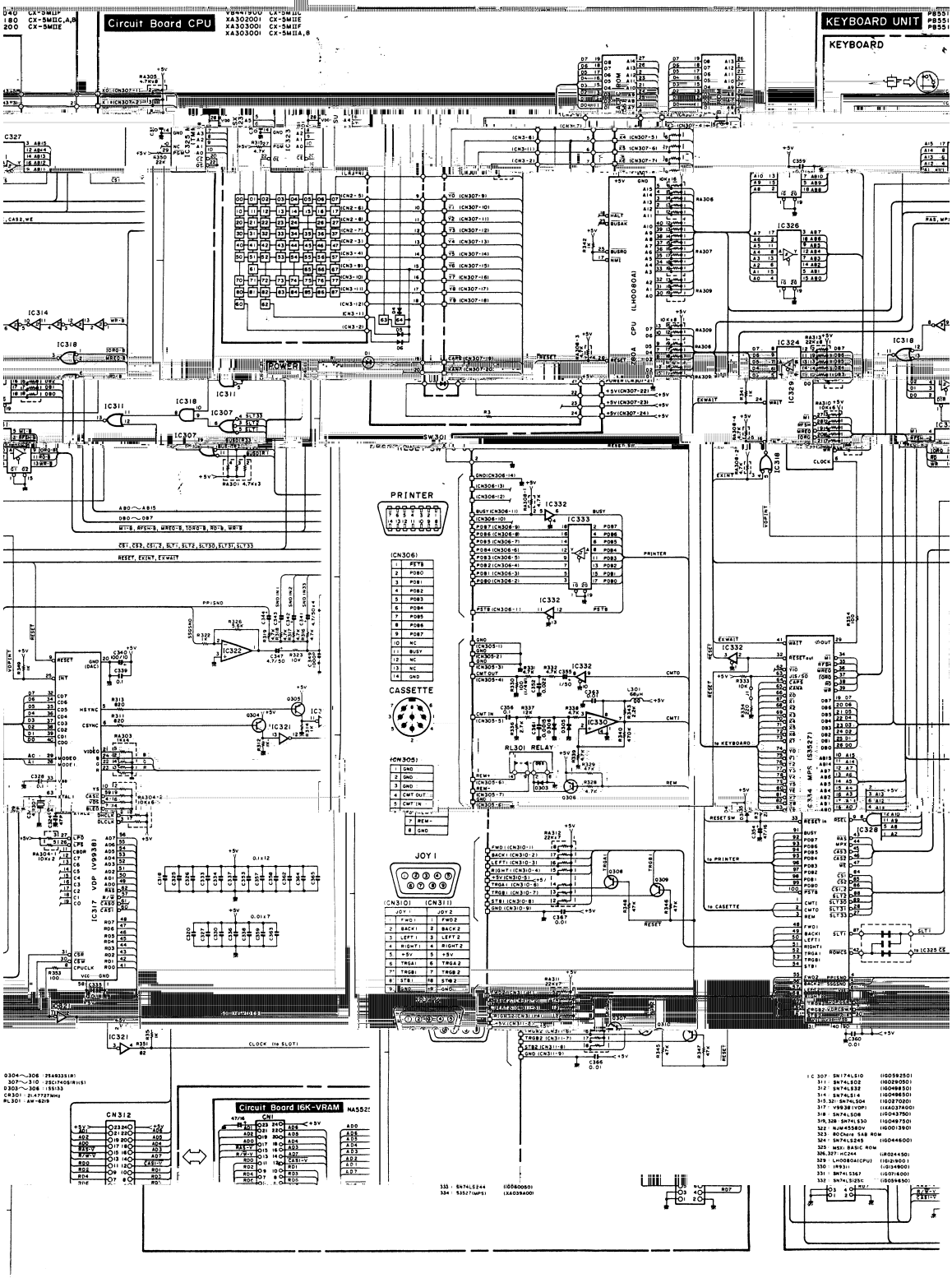


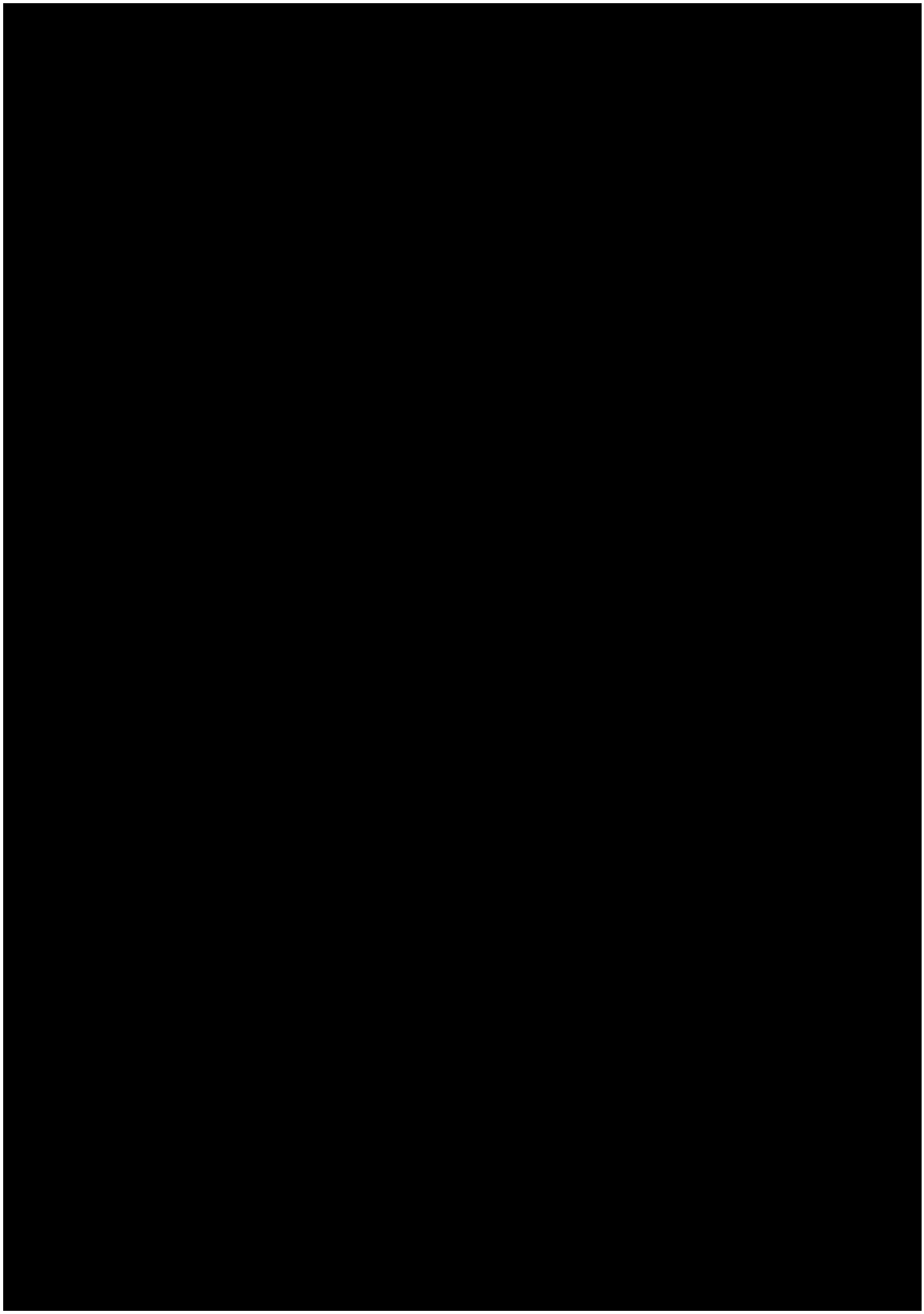


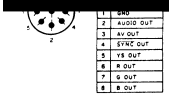
- DAC Diagram (YM3012)

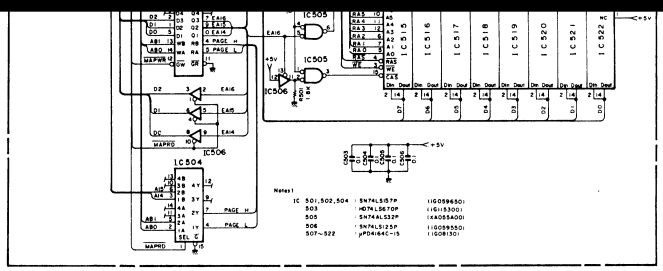


■ CX-5MII 64K/128 SCHEMATIC CIRCUIT DIAGRAM

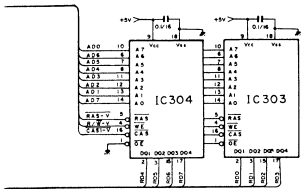




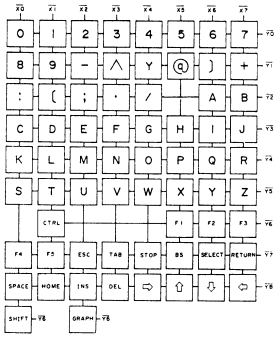


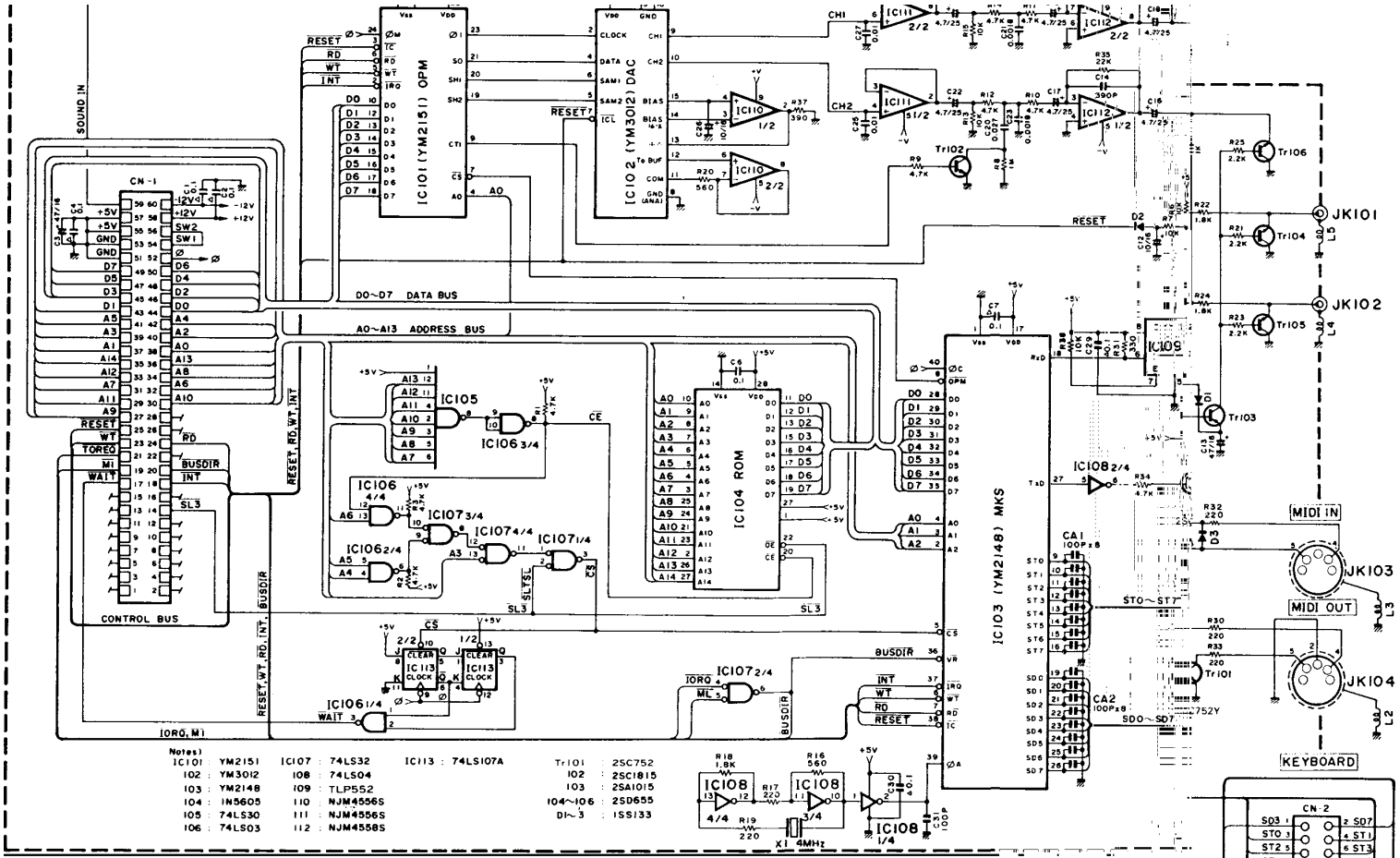


CPU VB441900 Video Circuit Canada

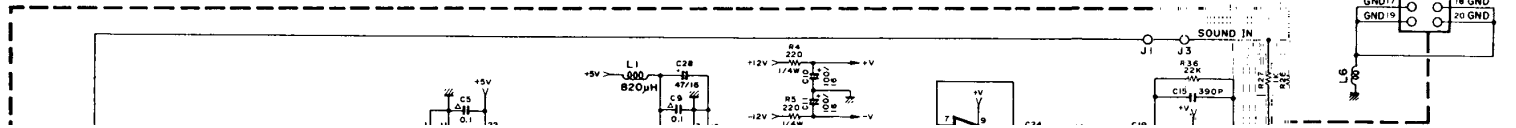


IC303, 304 : MB81416-12

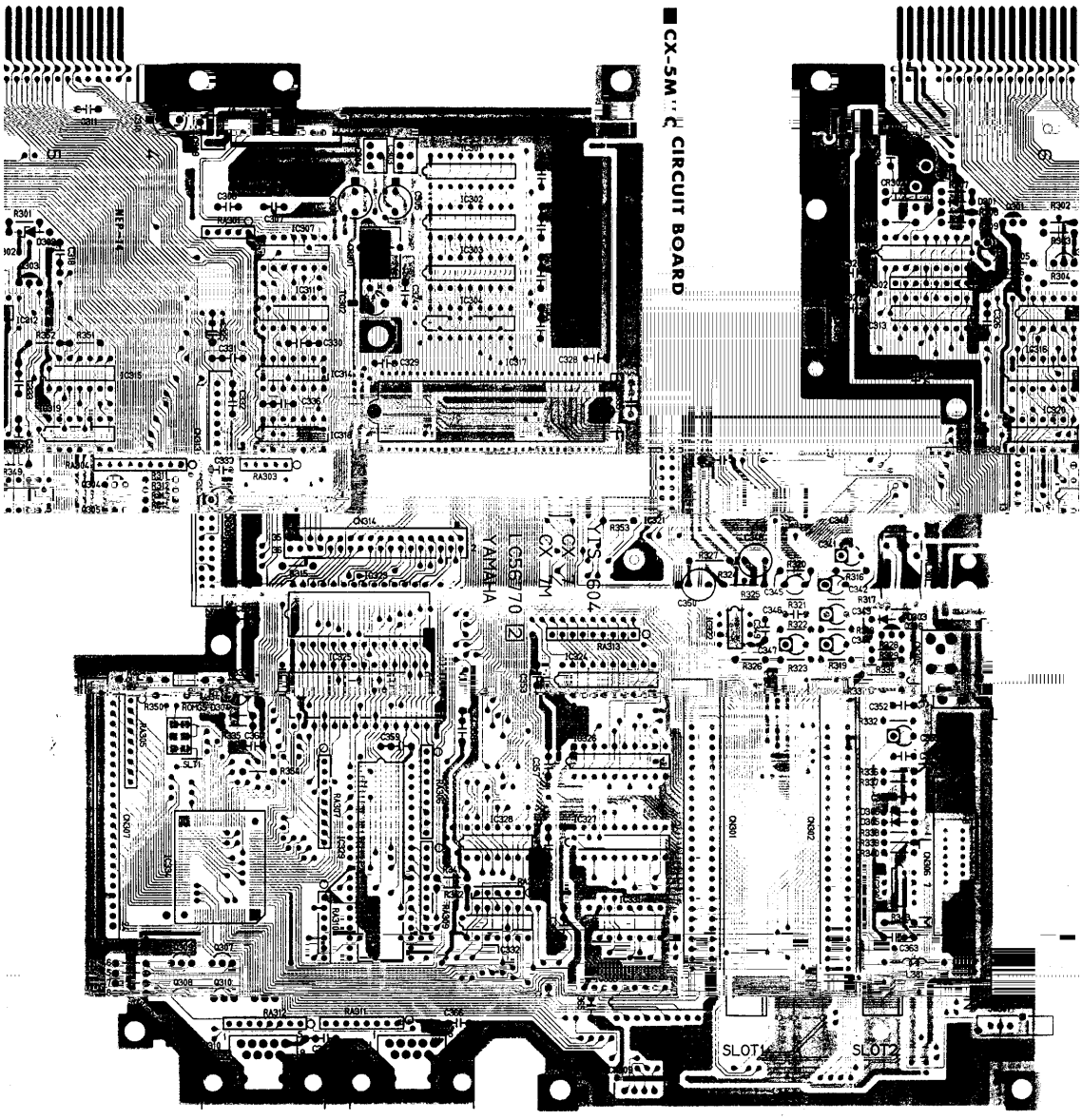




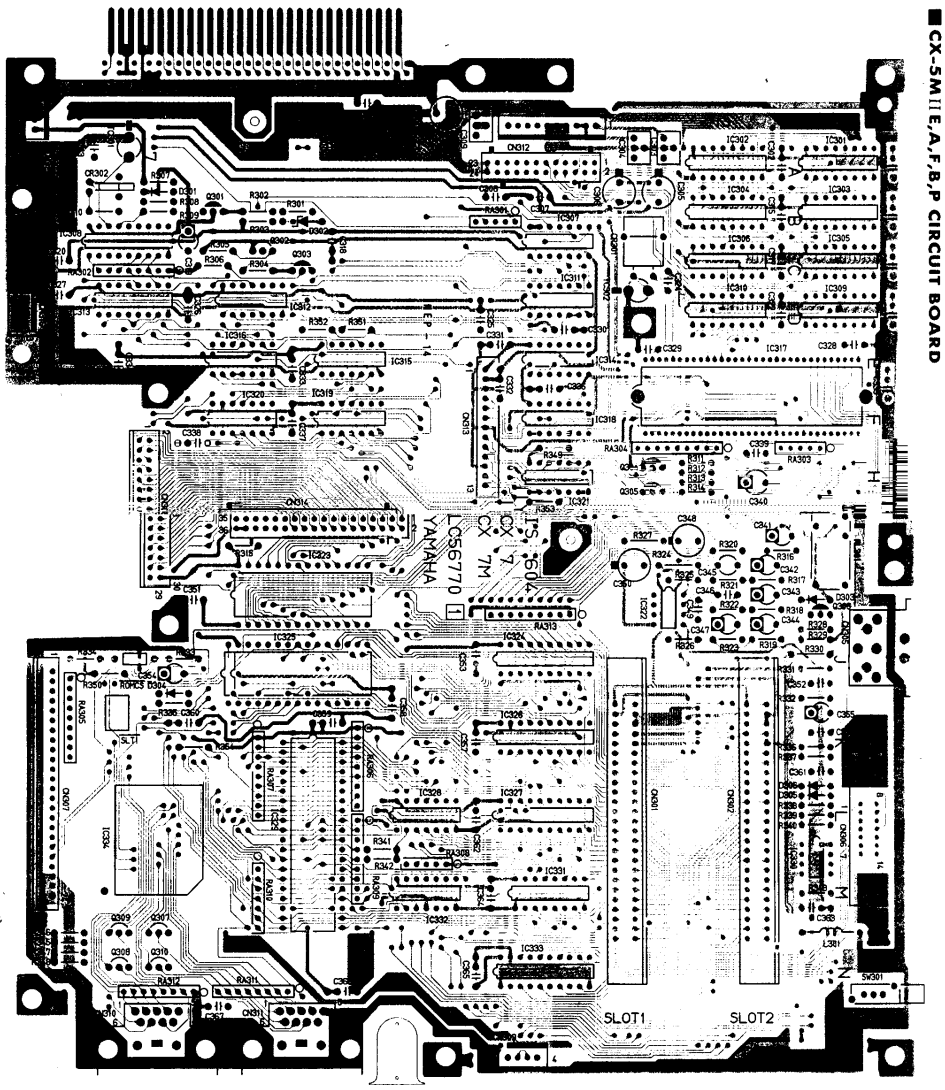
■ CIRCUIT BOARD (FM SOUND UNIT)



■ CX-5M [illegible] CIRCUIT BOARD

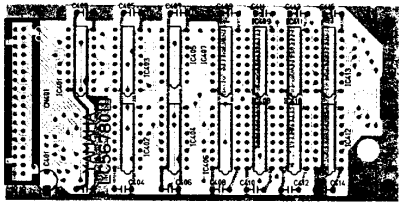


■ CX-5MIIE,A,F,B,P CIRCUIT BOARD

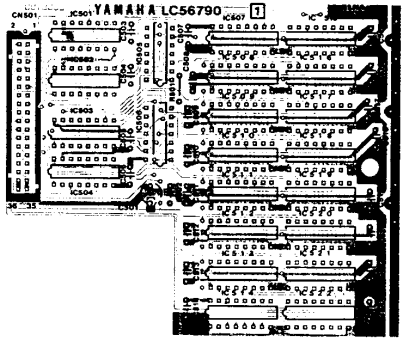


■ 16K V-RAM CIRCUIT BOARD

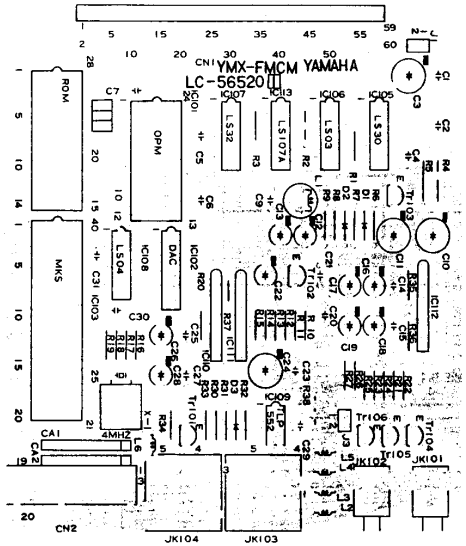
■ 64K DRAM CIRCUIT BOARD



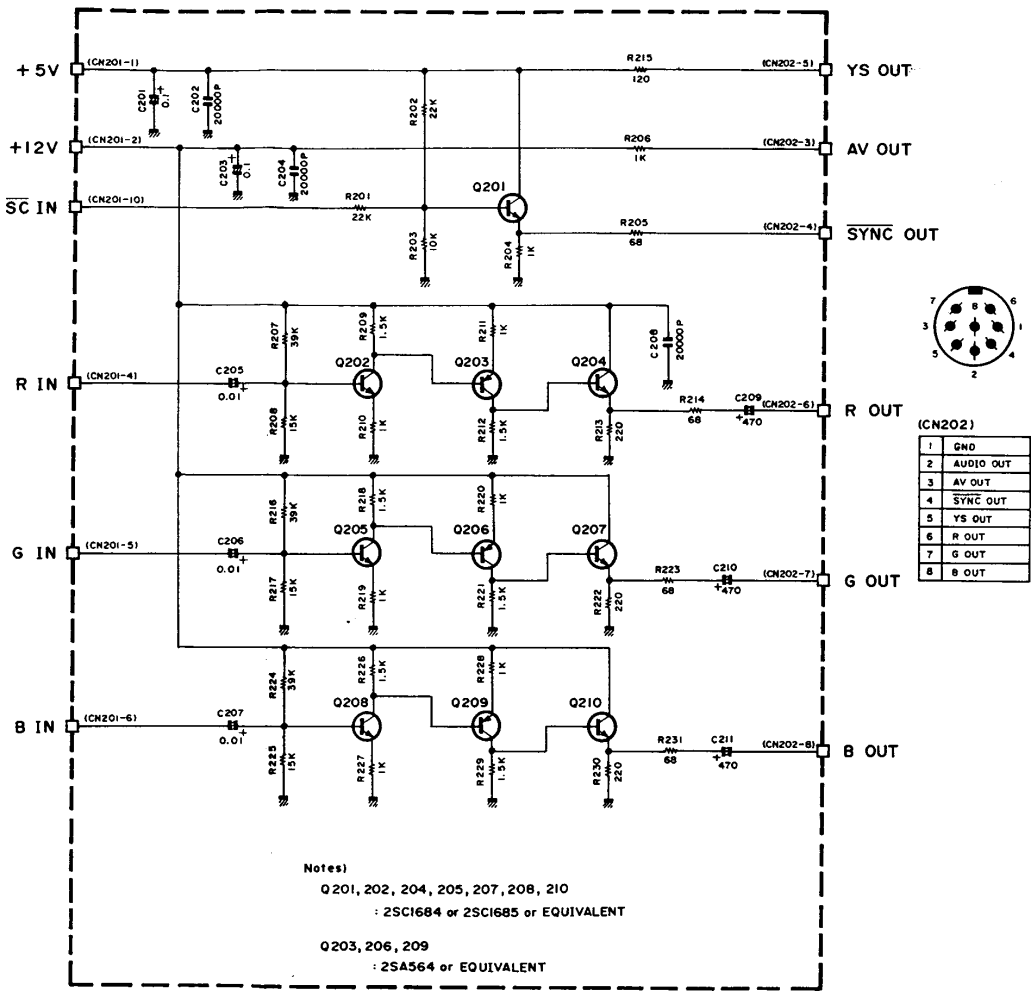
■ 128K DRAM CIRCUIT BOARD WITH MAPPER



■ CIRCUIT BOARD (FM SOUND UNIT)



● PB551150 (CX-5M II F) old



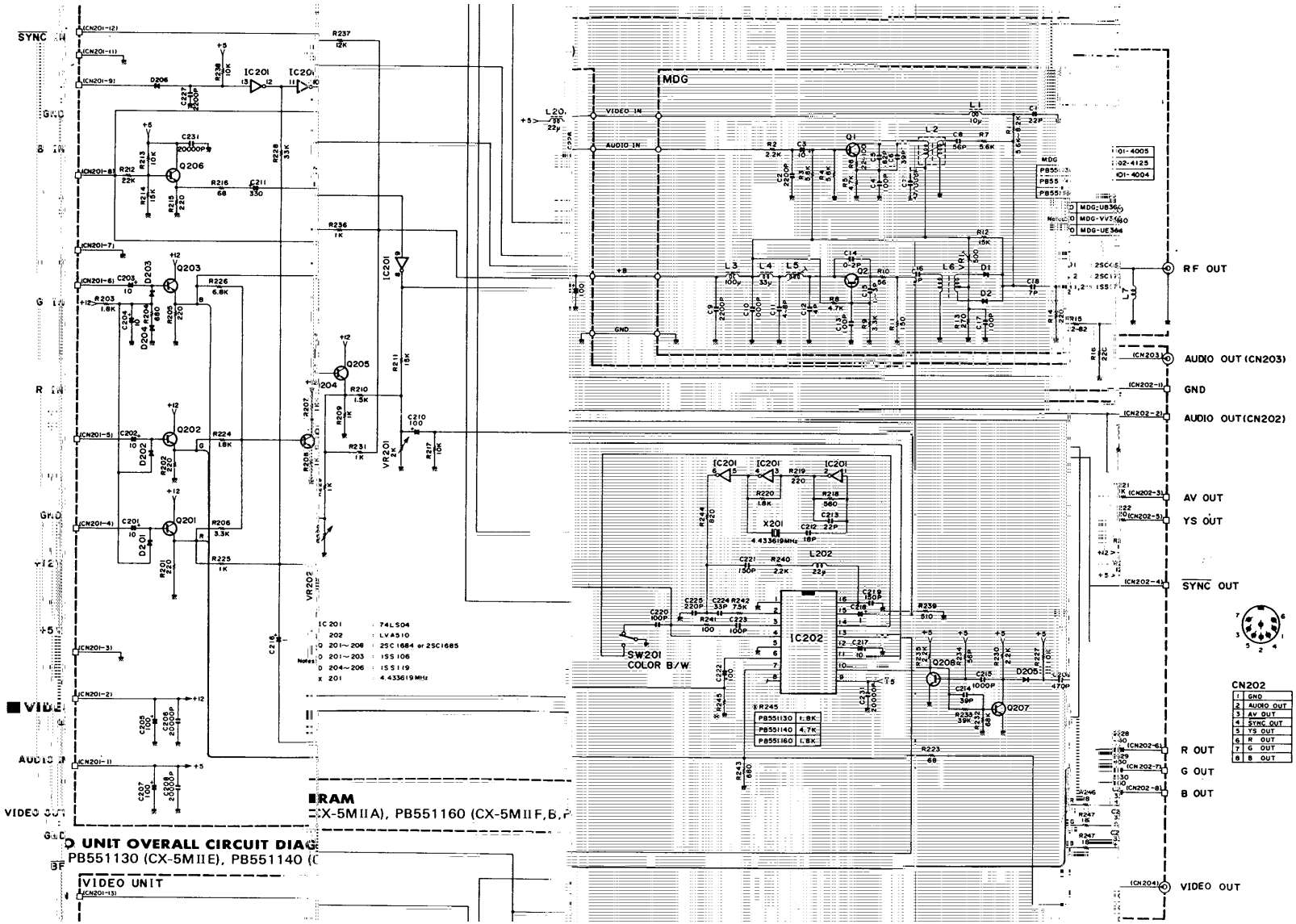
(CN202)

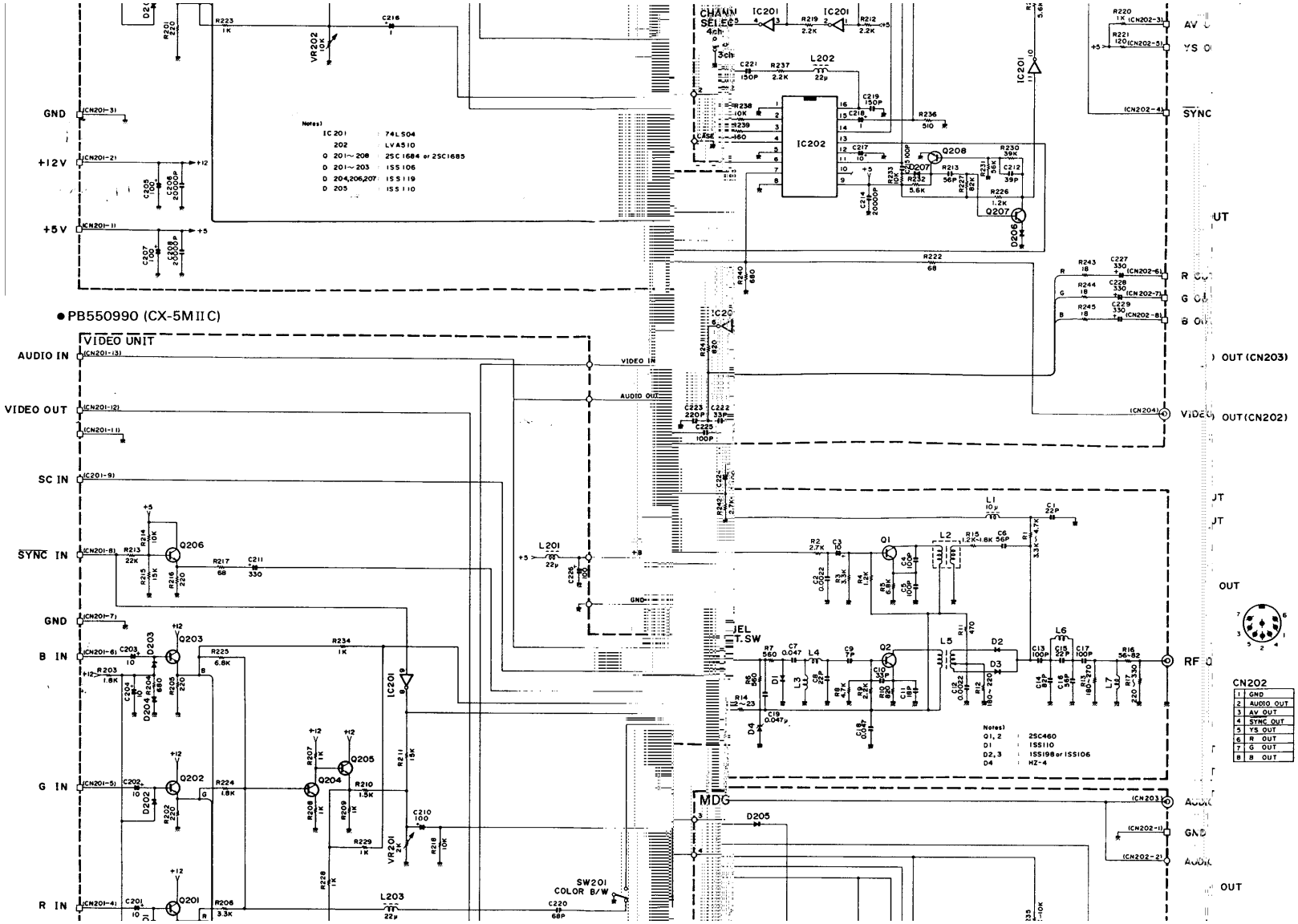
1	GND
2	AUDIO OUT
3	AV OUT
4	SYNC OUT
5	YS OUT
6	R OUT
7	G OUT
8	B OUT

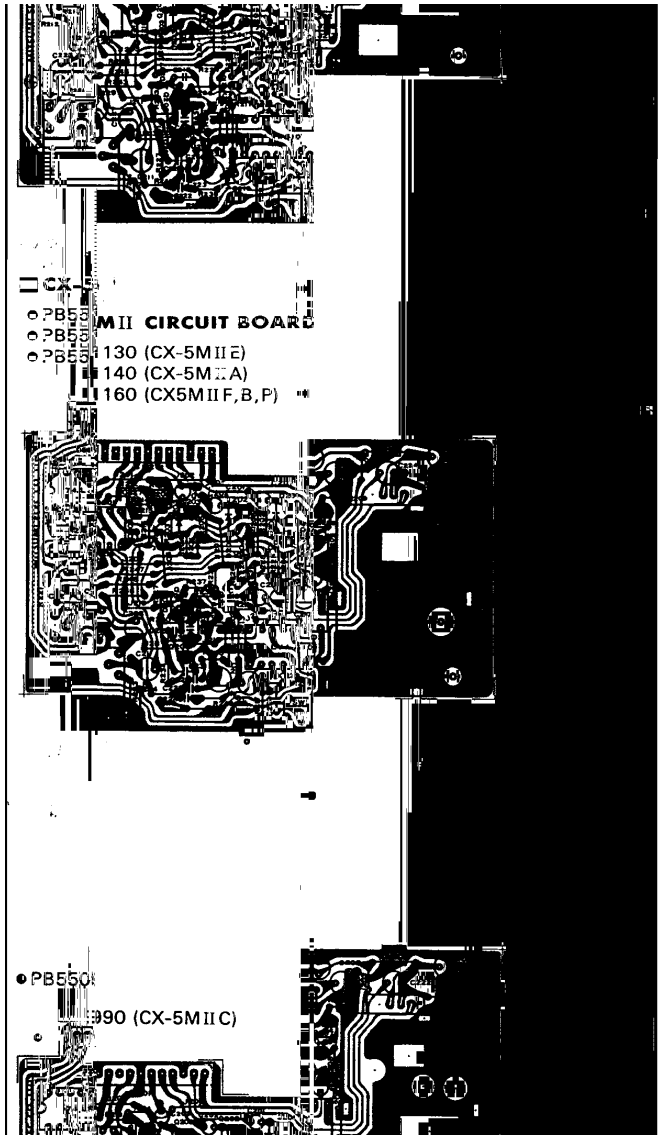
Notes)

Q201, 202, 204, 205, 207, 208, 210
: 2SC1684 or 2SC1685 or EQUIVALENT

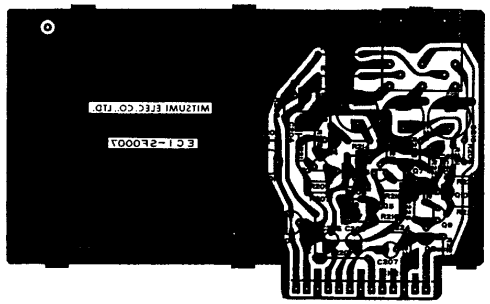
Q203, 206, 209
: 2SA564 or EQUIVALENT


MDG
VIDEO IN
AUDIO IN
GND
+B
RF OUT
AUDIO OUT (CN203)
GND
AUDIO OUT(CN202)
AV OUT
YS OUT
SYNC OUT
R OUT
G OUT
B OUT
VIDEO OUT
SW201
COLOR B/W
IC202
X201
4.433619MHz
Q205
Q206
Q207
Q208
CN202
1 GND
2 AUDIO OUT
3 AV OUT
4 SYNC OUT
5 YS OUT
6 R OUT
7 G OUT
8 B OUT
VIDEO UNIT
PB551130 (CX-5MIIE), PB551140 (
RAM
X-5MIIA), PB551160 (CX-5MIIF,B,
UNIT OVERALL CIRCUIT DIAG


● PB550990 (CX-5M II C)
VIDEO UNIT
AUDIO IN
VIDEO OUT
SC IN
SYNC IN
GND
B IN
G IN
R IN
+12V
+5V
VIDEO IN
AUDIO OUT
MDG
SW201
COLOR B/W
IC201
IC202
L201
L202
L203
Q1
Q2
Q201
Q202
Q203
Q204
Q205
Q206
Q207
Q208
D205
VR201
VR202
Notes)
IC 201 : 74LS04
202 : LV4510
Q 201~208 : 2SC1684 or 2SC1685
D 201~203 : 1SS106
D 204,206,207 : 1SS119
D 205 : 1SS110
Notes)
Q1, 2 : 2SC460
D1 : 1SS110
D2, 3 : 1SS198 or 1SS106
D4 : MZ-4
CN202
1 GND
2 AUDIO OUT
3 AV OUT
4 SYNC OUT
5 YS OUT
6 R OUT
7 G OUT
8 B OUT

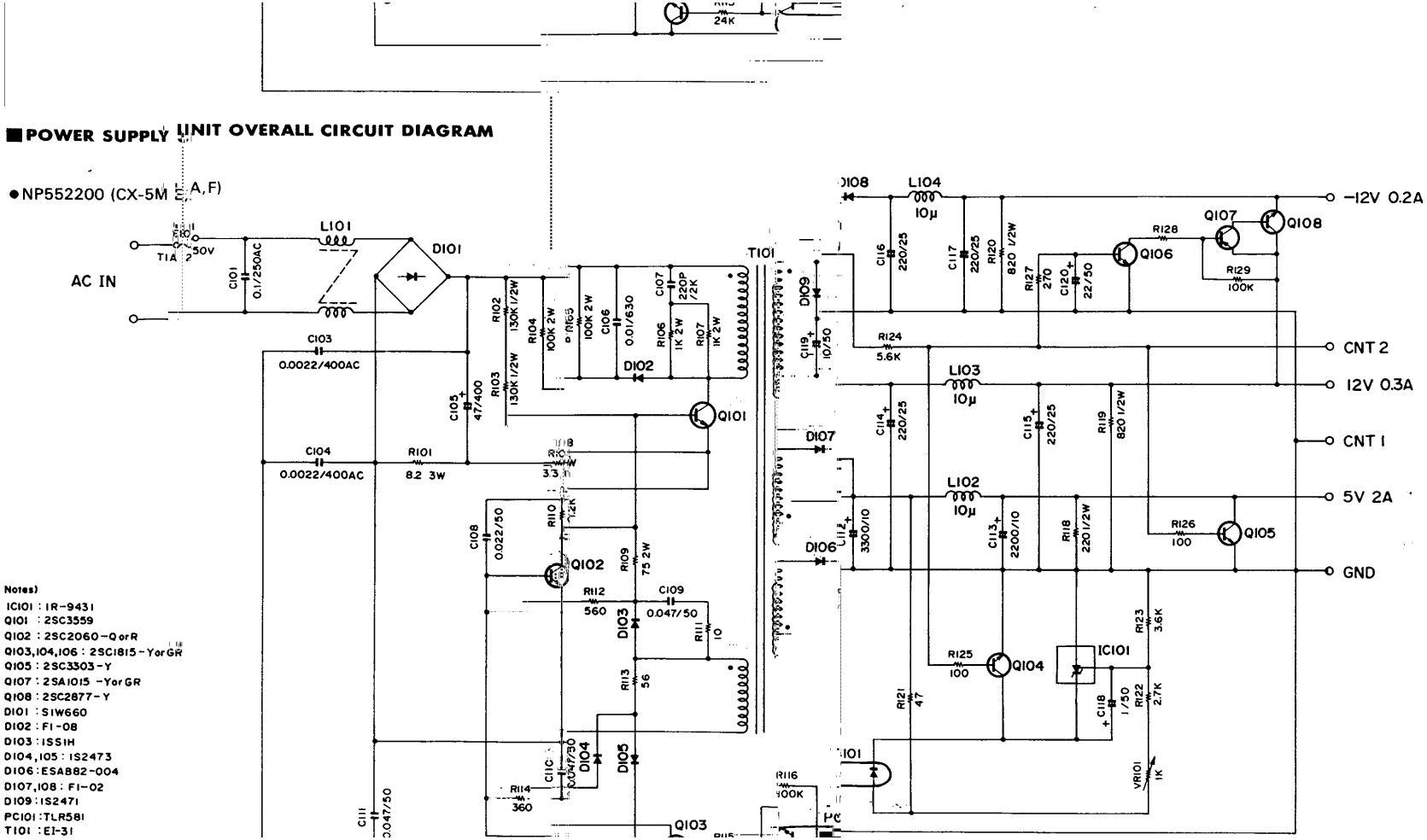


● PB551150 (CX5MIIF) old



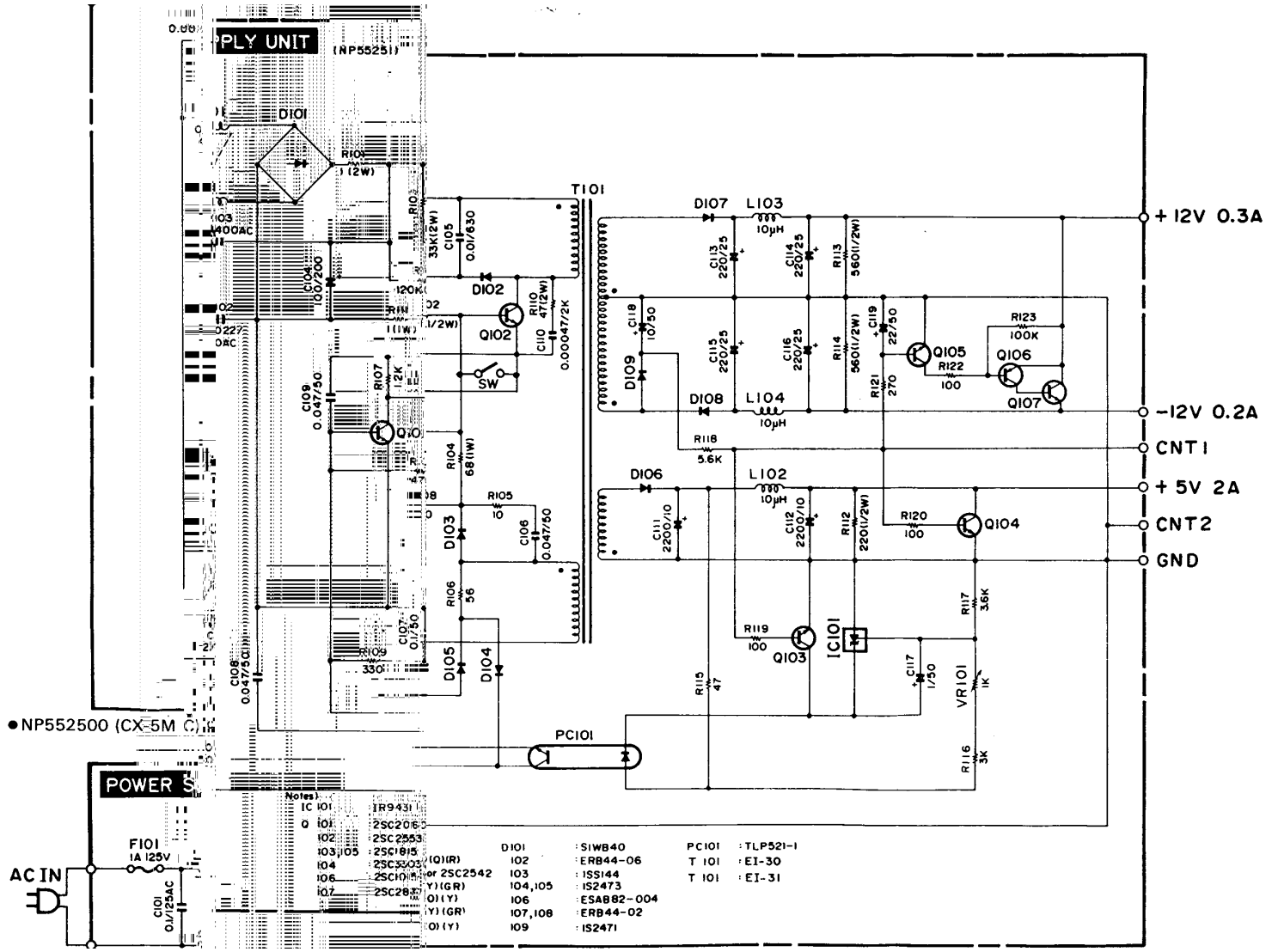
■POWER SUPPLY UNIT OVERALL CIRCUIT DIAGRAM

● NP552200 (CX-5M [illegible] A, F)



Notes)

IC101 : IR-9431
Q101 : 2SC3559
Q102 : 2SC2060-Q or R
Q103,104,106 : 2SC1815-Y or GR
Q105 : 2SC3303-Y
Q107 : 2SA1015 -Y or GR
Q108 : 2SC2877-Y
D101 : S1W660
D102 : FI-08
D103 : 1SS1H
D104,105 : 1S2473
D106 : ESAB82-004
D107,108 : FI-02
D109 : 1S2471
PC101 : TLR581
T101 : EI-31


PLY UNIT
(NP5525)
D101
T101
D107
L103
10µH
+12V 0.3A
D102
Q102
SW
D109
D108
L104
10µH
-12V 0.2A
CNT1
D106
L102
10µH
+5V 2A
CNT2
GND
Q105
Q106
Q107
Q104
Q103
IC101
PC101
VR101
D103
D105
D104
Q101
R104 68(1W)
R105 10
R106 56
R107 1.2K
R109 330
R110 47(2W)
R111 560(1/2W)
R112 220(1/2W)
R113 560(1/2W)
R114 560(1/2W)
R115 47
R116 3K
R117 3.6K
R118 5.6K
R119 100
R120 100
R121 270
R122 100
R123 100K
C101 0.1/125AC
C102 0.022/250AC
C103 0.1/400AC
C104 100/200
C105 0.01/630
C106 0.047/50
C107 0.1/50
C108 0.047/50
C109 0.047/50
C110 0.00047/2K
C111 2200/10
C112 2200/10
C113 220/25
C114 220/25
C115 220/25
C116 220/25
C117 1/50
C118 10/50
C119 22/50
F101 1A 125V
AC IN
● NP552500 (CX-5M C)
POWER S
Notes)
IC 101 : IR9431
Q 101 : 2SC2063
102 : 2SC2553
103,105 : 2SC1815
104 : 2SC3503 (Q)(R)
106 : 2SC1815 or 2SC2542
107 : 2SC2814 (Y)(GR)
(Y) : 2SA1015 (Y)
(Y)(GR) : 2SA1015 (Y)(GR)
(Y) : 2SA1015 (Y)
D101 : S1WB40
102 : ERB44-06
103 : 1SS144
104,105 : 1S2473
106 : ESAB82-004
107,108 : ERB44-02
109 : 1S2471
PC101 : TLP521-1
T 101 : EI-30
T 101 : EI-31

-P)

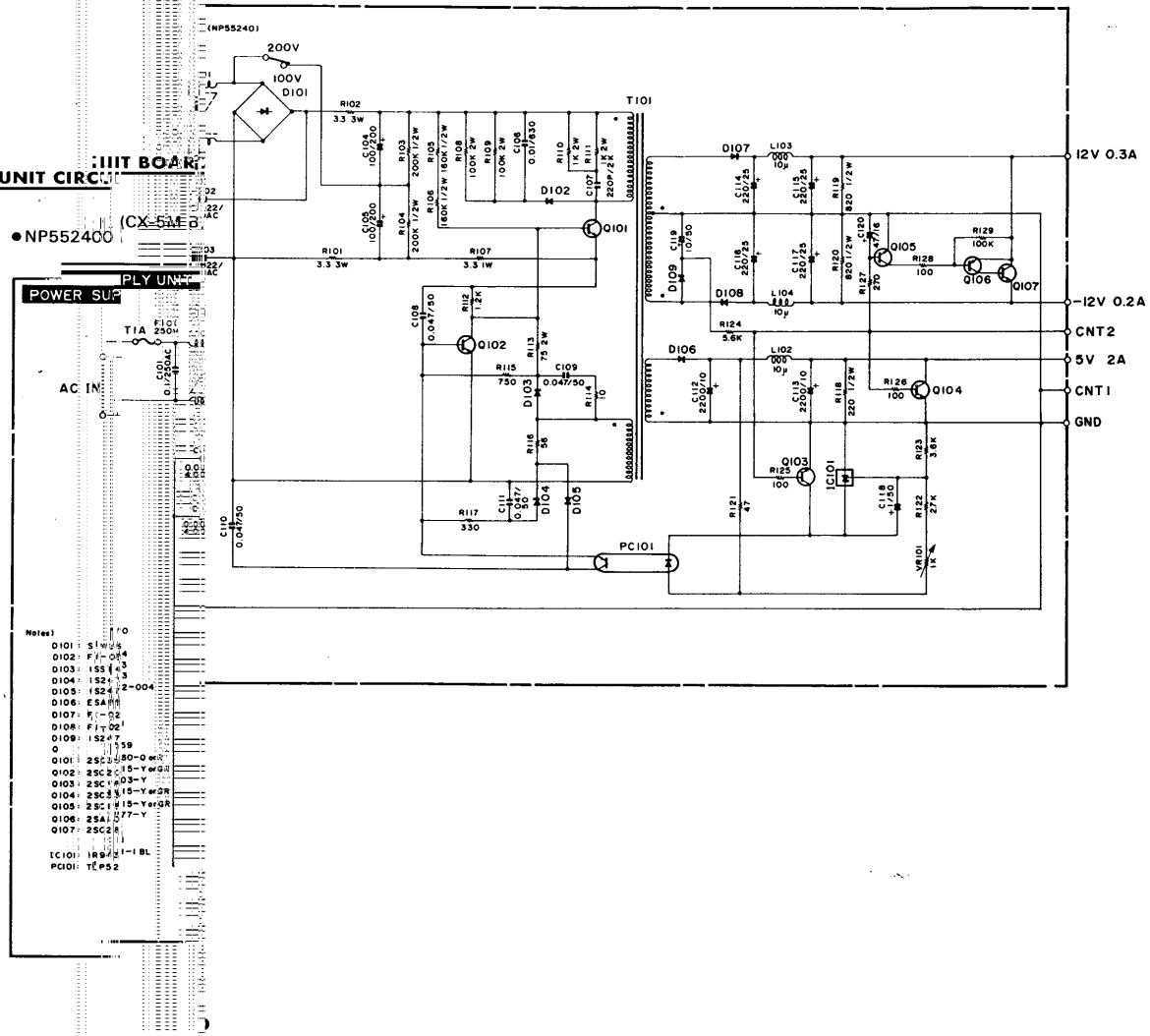
SUPPLY UNIT CIRC[illegible] BOARD

(CX-5MKII)

●NP552400

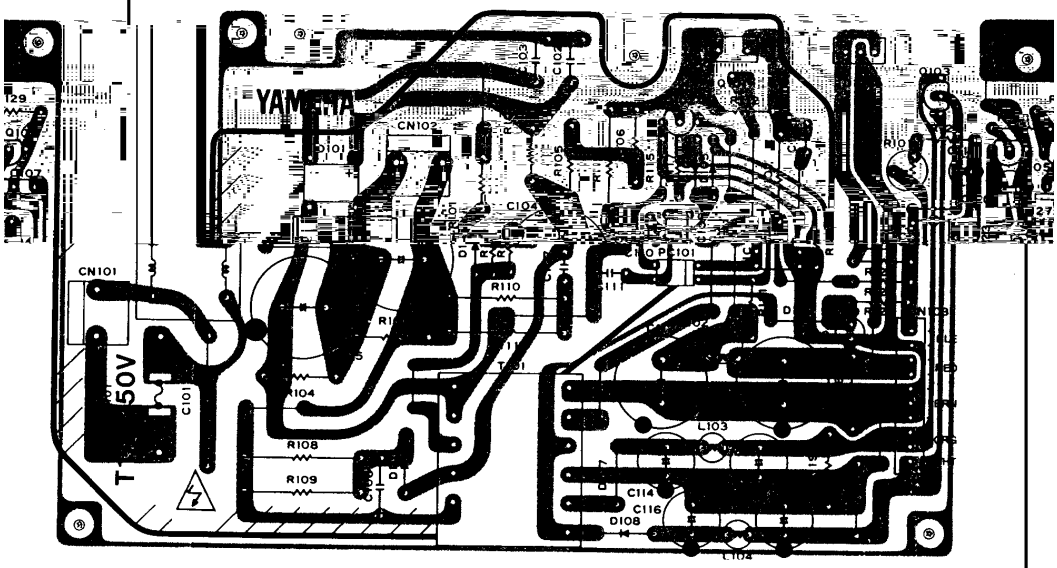
PLY UNIT

POWER SUP



■ POWER SUPPLY UNIT CIRCUIT BOARD

● NP552400 (CX-5M B,P)



● NP552500 (CX-5M C)